UNIVERSIDADE TECNOLÓGICA FEDERAL DO PARANÁ

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CONVERSOR BUCK-BOOST INTERLEAVED COM MODULAÇÃO EM FREQUÊNCIA APLICADO A CORREÇÃO DE FATOR DE POTÊNCIA

CURITIBA

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Interleaved Buck-Boost Converter with Frequency Modulation Applied in Power Factor Correcting

Dissertação de mestrado apresentado como requisito para obtenção do título de Mestre em Engenharia Elétrica do Programa de pós graduação em engenharia elétrica e informática industrial da Universidade Tecnológica Federal do Paraná.

Orientador: Doutor Alceu André Badin

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Trabalho de pesquisa de mestrado apresentado como requisito para obtenção do título de Mestre Em Ciências da Universidade Tecnológica Federal do Paraná (UTFPR). Área de concentração: Engenharia De Automação E Sistemas.

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Dedico este trabalho a minha família e aos
meus amigos, pelos momentos de ausência.

RESUMO

Esse trabalho propõe uma nova célula de comutação aplicada a um conversor Buck-Boost CA-CC, com modulação pulse-frequency (PFM), usada como corretor de fator de potência (PFC), com comutação suave e sem problemas de recuperação reversa. Esse conversor apresenta, devido a sua modulação (PFM), a característica de um seguidor de tensão com distorção proporcional a sua saída de tensão, isso da a vantagem ao conversor de não precisar de um loop de controle de corrente. Essa dissertação apresenta o principio de operação, uma analise matemática do conversor e os resultados práticos de um conversor de 1 kW Buck-Boost em modo de condução continua (CCM), em conjunto com uma analise normativa de sua distorção harmônica de acordo com a IEC 61000-3-2.

Palavras-chave: conversor ca-cc; buck-boost; sfm; comutação suave; seguidor de tensão.

ABSTRACT

This work proposes a new switching cell applied at a AC-CC buck-boost converter with switching frequency modulation (SFM) used as a power factor corrector (PFC), Soft-switching and no reverse recovery time problems are achieved with SFM. This converter presents, due to the SFM, the characteristics of a voltage follower with a distortion proportional to the output voltage, this gives the converter the advantage of not needing a current loop. This thesis presents the operating principle, a mathematical analysis of the converter and the practical results of a 1 kW buck-boost in continuous conduction mode (CCM), together with a normative analysis of its harmonic distortion according to the IEC 61000-3-2.
Keywords: converter ac-cc; buck-boost; sfm; soft commutation; voltage follower.

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1 INTRODUCTION

The AC-DC converter is widely used in electronic ballasts, power supplies, variable-speed ac motor drives, telecommunications power sources, etc. Due to regulation standards, most new applications require that the power factor of power sources reach certain levels of quality (ELECTROMAGNETIC. . . , 1995) -(IEEE. . . , 1992). These standards are created to preserve the energy quality, limiting the amount of harmonic distortion one can cause. Regulations also require power factor correction (PFC) topologies to limit the amount of reactive power an equipment can demand from a power grid.

Electronic devices are, by and large, equipment that deteriorates the quality of the available energy. A converter that does not have a resistive characteristic and does not have a active control of its electrical current has a low energy quality, which translates to a low power factor (PF) and a high level of total harmonic distortion (THD), this can damage other equipment connected to the same power source and cause losses in the energy distribution. Due to those reasons regulation standards were created, so most new applications require that the power factor of power sources reach certain levels of quality (ELECTROMAGNETIC. . . , 1995) -(IEEE. . . , 1992) These standards are created to preserve the energy quality, limiting the amount of harmonic distortion one can emit also requiring power factor correction (PFC) topologies to limit the amount of reactive power an equipment can demand from a power grid.

The power factor is not only affected by the reactive power present but also by the harmonic distortion in the current and voltage and the energy stored in the load. A well-designed PFC must be able to solve these issues demanding from the source mostly active power(SAFWAT; XIAHUA, 2017); the PFC could be passive or active, but as shown in (SAFWAT; XIAHUA, 2017), to achieve normative standards, an active PFC is the best choice. The most commonly used AC-DC converters are buck converters, boost converters, and buck-boost converters.

In order to tackle the power factor (PF) and total harmonic distortion (THD) problems discussed before, this work proposes a new switching cell applied to an AC-CC buck-boost converter with pulse-frequency modulation (PFM) used as a power factor corrector (PFC).

1.1 Topology discussion

To better define a topology that could better suit the discussed problem a bibliography analysis was made, this analysis brought up that each topology of converters has its advantages and problems.

Starting with the buck converter, this is not an ideal choice as a PFC due to not naturally having a power factor that achieve the power factor standards; on the other hand, the boost converter can achieve the power factor standards quickly but can only step up the voltage level above its input. The buck-boost topology can also achieve the power factor standards and work with output voltages at least equal to input voltages, which makes it the best choice for the

chosen application. The boost PFC converter has wide acceptance due to its simple topology, high efficiency, and low cost. However, this converter presents problems with inrush current and high output voltage. The buck converter has a different problem. Despite having output voltages lower than the input, the buck converter presents issues with distortion of the input current in a part of the power cycle. On the other hand, the buck-boost PFC converter can increase and decrease the output voltage, present low distortion of the line current, and limit the inrush current at the start of the converter.(ZHAO; ABRAMOVITZ; SMEDLEY, 2015) However, this converter suffers from a large ripple in both input and output currents due to its discontinuous characteristic in source and load. This impacts the volume of filters and compromises efficiency, limiting their applications. (YARI; SHAHALAMI; MOJALLALI, 2021) An alternative to reduce this problem is to use an interleaving structure. (RANA; SONAR; BANERJEE, 2022) In this configuration, the converter reduces the ripple, dividing currents between the semiconductors and increasing the processed power.

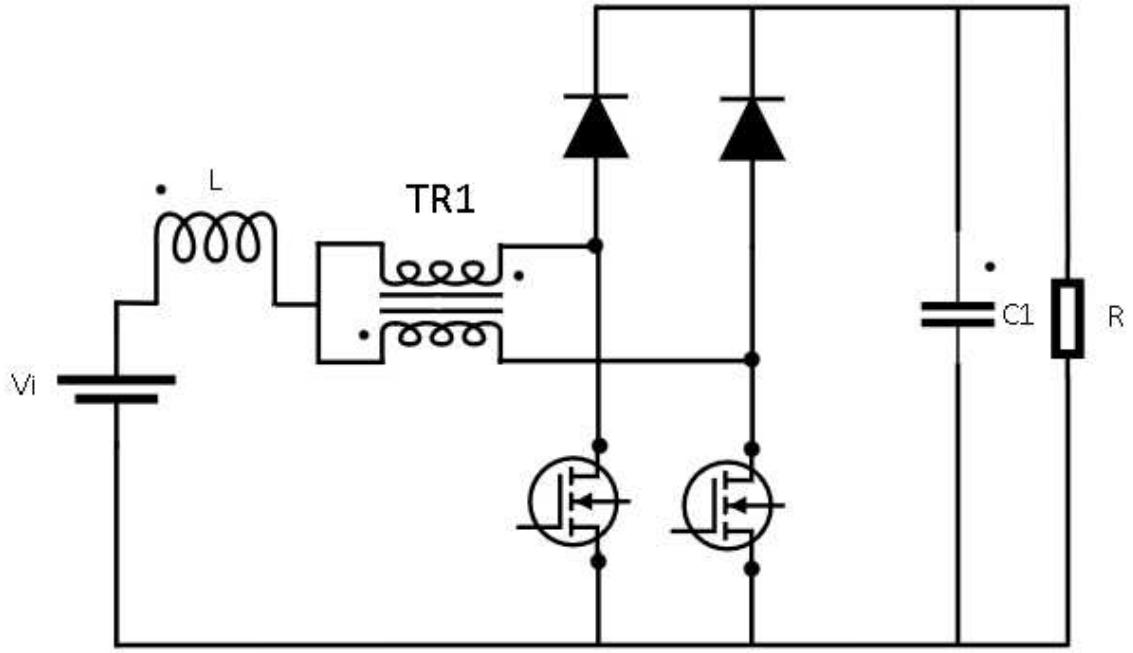
Several solutions are applied to reduce the stress on the semiconductors and enhance the converter's efficiency. As presented in (Hsieh; Hsueh; Yen, 2009), an interleaved topology that operates in a zero-voltage switching (ZVS) is one of the most applied techniques. Other options for achieving efficiency, such as other switching cells, can be found in studies such as (Bascope; Barbi, 2000) and (Feretti; Tofoli, 2017). In high-power applications, such solutions are very commonly applied to reach good efficiency levels, as seen in (Golkhandan; Ali Chamanian; Tahami, 2018).

Another critical aspect of PFC converters is the control strategies required for operation. Some topologies have a characteristic that the input current naturally follows the input voltage profile. (Simonetti; Sebastian; Uceda, 1997) This is observed in a few DC-DC converters. Most of those need to be operated in discontinuous conduction mode (DCM) to function as a voltage follower. Examples of those converters are Cuk (Simonetti; Sebastian; Uceda, 1997), Boost (Soares; Badin, 2021) and SEPIC (Simonetti; Sebastian; Uceda, 1997). This operational state brings the benefit of not needing a current loop, which can reduce cost by not requiring a current sensor and a powerful processor because the voltage controller is much slower than the current one. Eliminating the need for a current sensor also reduces the circuit's complexity, which is a very advantageous feature that the voltage follower display. These advantages are considered in several applications; one of the most common is power factor correction (PFC), as seen in (Peres; Martins; Barbi, 1994) and (Erickson; Madigan; Singer, 1990). Nevertheless, topologies working on DCM present higher peak currents and less efficiency in a higher power than those seen in CCM (Navamani *et al.*, 2015), which could be a problem and should be considered when choosing a topology to work on.

One of the main inspirations for the converter that will be presented throughout this thesis is the variation of the Boost converter presented in (Soares; Badin, 2021), Fig. (1) shows the converter. This topology share a lot of similarities with the proposed converter, making use of the same switching cell, but in a buck-boost topology. The main advantages seen in the Boost

variation are: Zero Voltage Switching (ZVS), partial Zero Current Transitions (ZCT), lower efforts on the semiconductors due to having 2 arms and the voltage follower characteristics, were a current loop in not necessary. The principal disadvantage is the impossibility of a output voltage lower than the input voltage, which makes so harder to use in lower voltage applications, without a lowering step before its load.

Figure 1 – Boost variation applying a switching cell

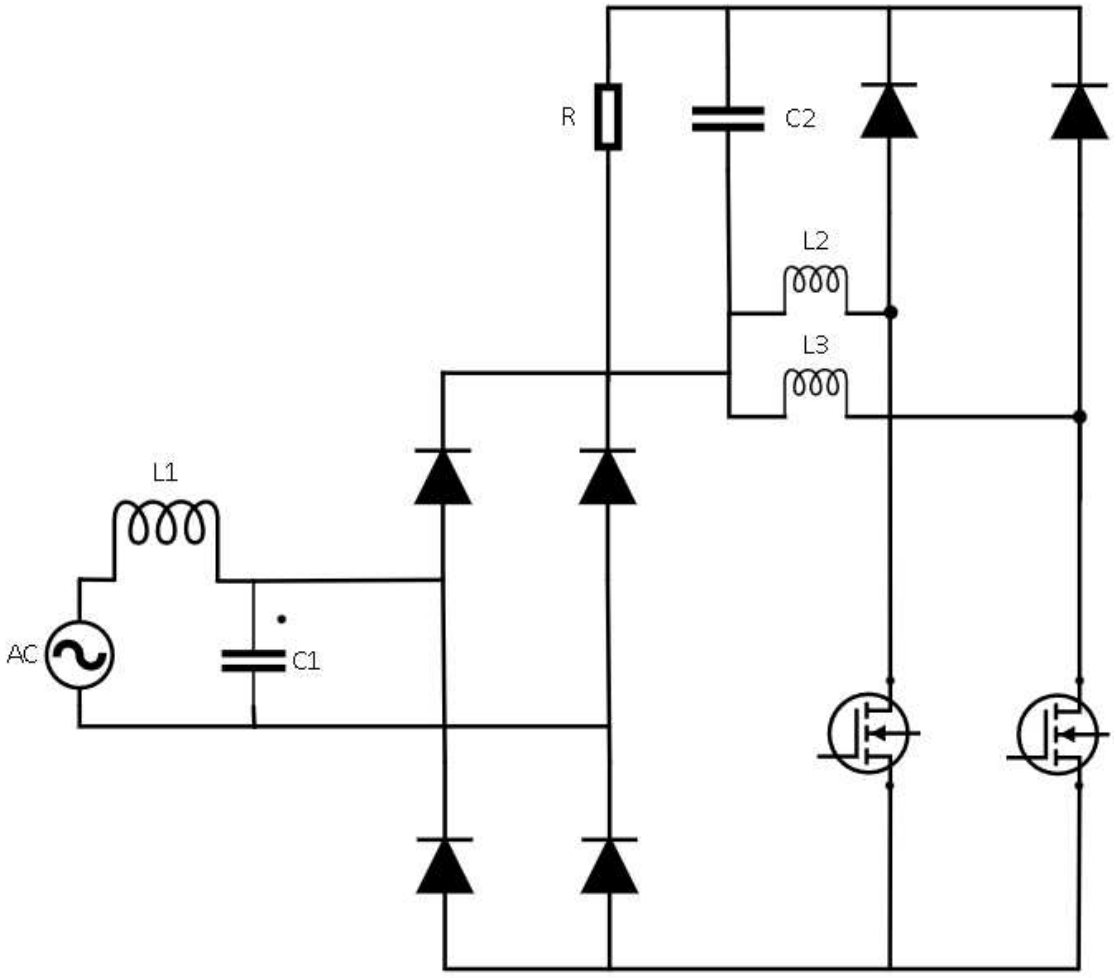


Source: Based on (Soares; Badin, 2021)

Another topology that was analysed as a basis to the proposed one is the conventional interleaved buck-boost presented in Fig. 2. This converter has several advantages: the buck-boost characteristics of being able of working with an output voltage lower or higher than its input voltage. Due to its second switching arm, it has lower current levels in each switch, diodes and inductors, reducing the building specifications for each component. Nevertheless this converters main drawbacks are: the losses presenting in switching, since the converter do not present the ZVS or ZCS characteristics, its necessity of a current loop for the output power control, this can be seen in (NAIR; LAKSHMINARASAMMA, 2020), if the voltage follower characteristic would be applied in this converter that would be a necessity of maintaining its operation mode in DCM as seen in (SIVANAGARAJU *et al.*, 2017), making so that the peak current on each component be higher, which would open the necessity for more robust components that are more costly.

This thesis proposes an interleaved buck-boost converter that applies a switching cell with frequency modulation (PFM). This topology approach presents several advantages when comparing it with other topologies, such as lower complexity than seen in (XUE; LEE, 2015), (XU *et al.*, 2022), (CONG; LIU; LEE, 2019), (ZHANG; CHENG; YIN, 2021), (WANG *et al.*, 2015) and (LIU *et al.*, 2021); a very simplified control when compared to topologies as (TIAN *et al.*,

Figure 2 – Buck-Boost variation applying a switching cell



Source: Based on (SIVANAGARAJU *et al.*, 2017; NAIR; LAKSHMINARASAMMA, 2020)

2022), (KIM *et al.*, 2019), (ZHENG *et al.*, 2016) and (RESTREPO *et al.*, 2020); the lack of need of a current control loop. It presents ZVS and a zero current and zero voltage transition (ZCZVT) in some steps of its operation, going even further in efficiency. Other outstanding features of the proposed converter are: - High power factor without current or input voltage sensors (no current loop is needed). - soft switching and without reverse recovery loss in diodes; - auto-balance of currents between the semiconductors; As stated before similar approach is presented by (Soares; Badin, 2021) and (SOARES; BADIN, 2022), who analyze the switching cell on a boost PFC converter. Furthermore, a double modulation is proposed to control and reduce the output voltage with the limitation of the switching frequency variation.

The rest of the paper is organized as follows. The proposed converter's topology and operation principles are described in Sections II and III. Section IV, presents the Current Zero Crossing Distortion passage. Section V presents the control strategy. Section VI shows the experimental results and the conclusions are given in Section VII.

1.2 Objectives

Develop a single-phase CA-CC PFC converter, with a switching cell, for applications that require more than 1kW in power output, this converter has to have:

- More than 95% efficiency;
- The harmonic values all below the standard EC 61000-3-2;
- Power Factor above 0.99.

1.3 Specific Objectives

In order of achieving the main objective, that is the study and development of a interleaved buck-boost converter using a switching cell with high frequency modulation (SC-PFM), it will be necessary:

- Study the the characteristics of the chosen topology;
- Simulate the converter in order of analysing its behaviour;
- Make a mathematics model of the defined topology;
- Elaborate the control strategy of the closed loop converter;
- Create a prototype and analyse its behaviour;

1.4 Contributions

This thesis intends to contribute with the study of AC-CC single-phase PFC converters by analysing the principle of operation of the proposed converter with the use of SFM and a switching cell.

1.5 Thesis arrangement

In this chapter it was shown different applications of AC-CC converters, presenting their main advantages and disadvantages, the main characteristics of the studied converter were also presented. Complementing the chapter the objectives and its contribution were also defined.

In the second chapter it is described the principle of operation and the mathematical equations that represent the converter, describing its process and the necessary knowledge to define the needed components of the circuit.

Chapter three explains the control strategy and presents one of the main advantages of this converters topology. Also presenting the code used in this converter.

Chapter four presents the experimental results that were obtained with the prototype, making so a complete analysis of its harmonic distortion, power factor and efficiency.

Finally chapter five presents the conclusions obtained with this thesis.

2 PROPOSED CONVERTER

This chapter will present the converter analysis, explaining: the converter switching cell; the proposed converter components; the converter operation and the converter current zero crossing distortion.

2.1 Converter Switching Cell

The converter switching cell is defined as a residual circuit when the power source and the load are removed, creating so a third state to the usual two state converters (PIETKIEWICZ; TOLLIK, 1984). The main objectives in utilizing this switching cell are:

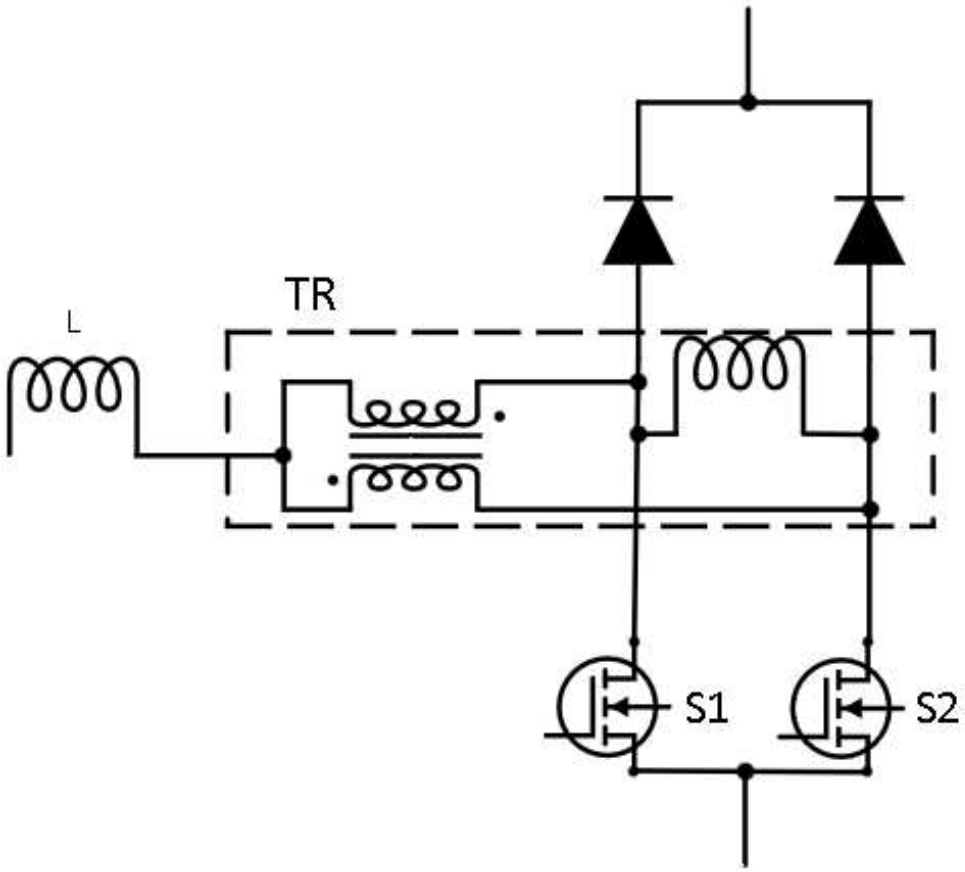
- Reducing the switching losses by achieving, ZVT and partially ZCVT.
- Obtaining the characteristics of a voltage follower with PFM.

The reduced losses in commutation result in smaller heat sinks, which makes the converter smaller in size and weight. The voltage follower characteristics makes the controller simpler bringing the converter even more advantages.

The switching cell that was used on the proposed topology is shown on the converter in Fig. 3. The switching cell has two arms with two switches, two diodes, an inductor and an auto-transformer TR, which has an unity turns ratio. The transformer connects with the two arms of the switching cell and has its magnetizing inductance represented by the inductor L_m between the switches S_1 and S_2. Because it has two times the magnetizing inductance measured in one winding of the transformer it is represented as L_m. The magnetizing inductance is very important to the commutation process due to the fact that its magnetic field bring the current to a point of inertia that unblocks the diodes current in between switches making the switching process ZVT.

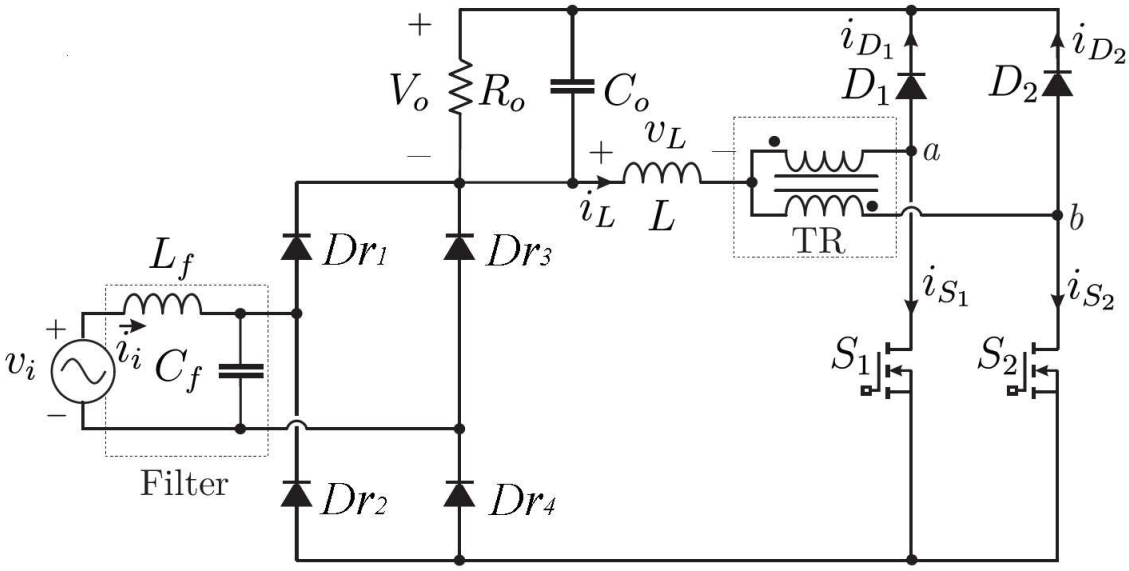
The switching cell works based on the complementary operation of both switches that are connected to a common node. While one switch conducts current, the other stay blocked. The only other option that the switching cell presents is leaving both switches blocked, leaving the converter unable to process power. With this analysis it can be defined that the switching cell is a three state switching cell. If the converter operation do not make use of this state of not processing power the conduction mode is continuous (CCM) if it does make use of it the conduction mode is discontinuous (DCM). The use of frequency modulation (PFM) makes so that the CCM characteristics of current peak can be applied together with a no power conduction state, that gives the voltage follower characteristics of the DCM conduction mode.

Figure 3 – Switching Cell configuration for PFM



Source: Author

Figure 4 – Proposed Converter



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2.2 Proposed Converter

The converter that will be proposed in this thesis is an interleaved buck-boost converter that applies a switching cell with frequency modulation (PFM), working as a rectifier and a power factor corrector. This topology is shown in figure 4. This converter is composed by a filter inductor and a filter capacitor, indicated as L_f and C_f, followed by a rectifying stage that is composed of four diodes. The converter presents a inductor refereed as L, an auto transformer refereed as TR, two switching arms, composed of a switch and a diode, refereed as S_1, S_2, D_1 and D_2. At last, the converter present a output capacitor refereed as C_0.

The converter analysis was made considering the following bases:

- Positive semi-cycle on the input voltage.
- No variation on the output voltage.

The buck-boost topology was chosen due to its versatility regarding its output voltage, that together with the switching cell, has the opportunity to work on several scenarios with simple control and few components.

2.3 Converter Operation

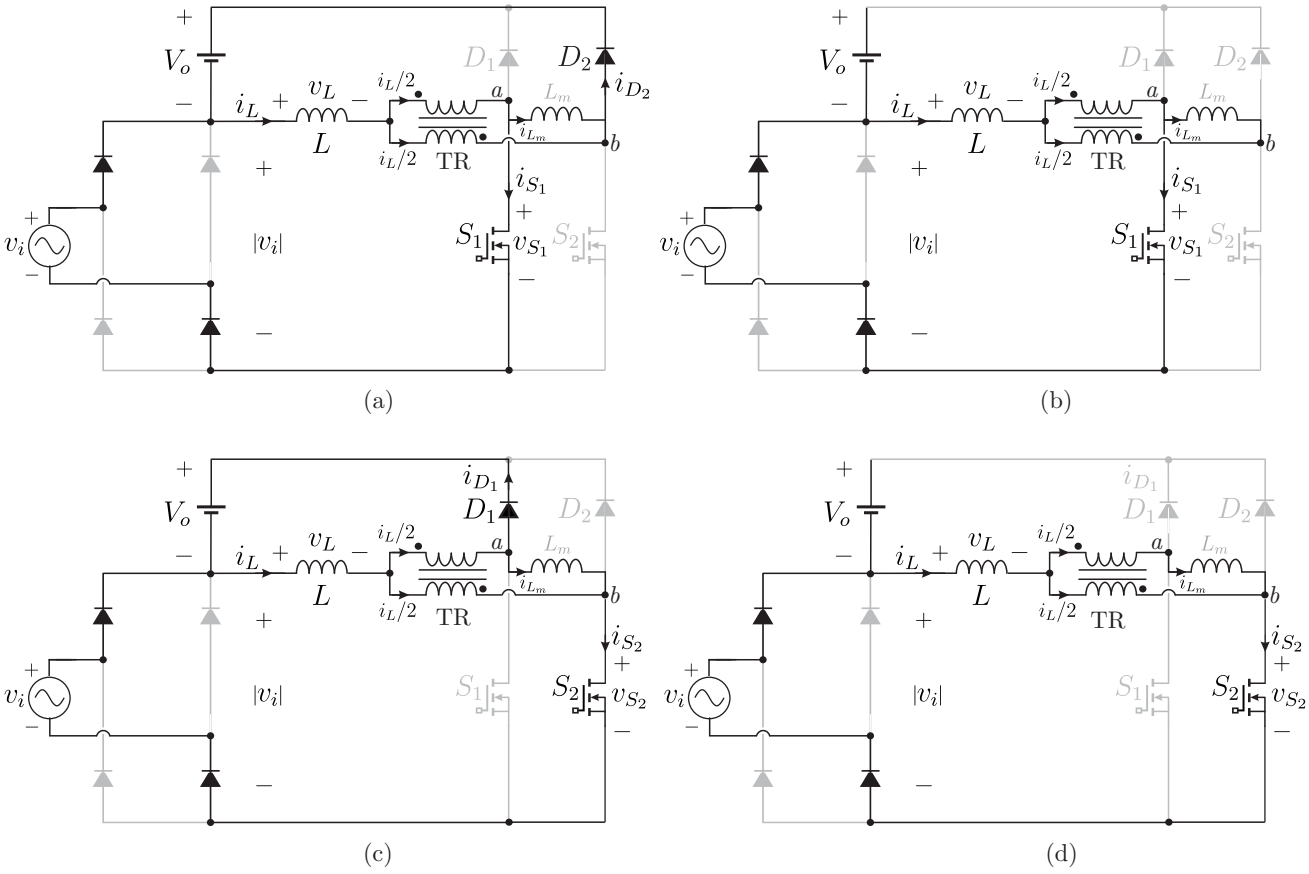
The converter will be presented with two voltage sources, V_i, that could also be presented as $V_p \cdot \sin(\omega t)$, and V_o, The output voltage V_o is considered constant, the conduction in L is CCM and its current is named I_L. Switches and diodes are ideal, except where the intrinsic diode and capacitance are taken into account. The transformer TR1 was separated into an ideal transformer and an external inductor L_m representing the magnetizing inductance; the current of inductor L is equally divided by the two windings of the transformer. The gates of switches S_1 and S_2 operate with fixed D = 0.5 and 180º phase shift; the circuit is controlled by PFM. The effective duty cycle is denoted as δ, it corresponds to the ratio of time that the inductor stores energy. The converter also have a filter represented by the inductor L_f and capacitor C_f.

The operational states of the studied topology are presented in Fig. 5. Fig. 6 shows the wave forms on its main components during the operational states.

Since the steps are cyclical and steps 3 and 4 are very similar to the first two steps, the steps 1 and 2 will be described in order to explain the converters operation. steps 3 and 4 only differ in current and voltage direction over the magnetizing inductance. As the filter inductor and capacitor will not affect the operational steps, they will not be considered in the analysis.

Step 1 (t_0– t_1): At instant t_0, the switch S_1 is turned on and S_2 is turned off and the diode D_2 starts conducting. Throughout t_0–t_1 the inductor L transfers energy through the diode D_2. The voltage V_L at inductor L is determined by (1), the voltage at the auto-transformer TR is viewed as the voltage at the inductor L_m which is –V_i.$\sin(\omega t)$-V_o, the current at each of the

Figure 5 – Operational steps; Step a the inductor L transfers energy to the resistor R through the diode D_2; Step b ZVT on the commutation occur and the inductor L stores energy; Steps c and d are similar to steps a and b.



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arms of the auto transformers, also viewed as the current on the inductor L_m is determined by (2). Between t_0 and t_1 there is a point in time with no power transferring. This point in time “ta” [4] is calculated by the voltage equation on the inductor L_m (3). "T"represents the converters switching period.

$$V_L = \frac{V_p \cdot \sin(\omega t) - V_o}{2}; 0 < t < ta \tag{1}$$

$$I_{Lm}(ta) = \frac{-I_L}{2}; I_{Lm}(0) = \frac{I_L}{2} \tag{2}$$

$$I_{Lm}(ta) = I_{Lm}(0) - \frac{1}{L_m} \cdot \int_0^{ta} (V_p \cdot \sin(\omega t) + V_o) dt \tag{3}$$

$$ta(\omega t) = T \cdot \frac{V_p \cdot \sin(\omega t)}{V_o + V_p \cdot \sin(\omega t)} \tag{4}$$

Step 2 (t_1–t_2): At time instant t1, diode D2 is in a blocked state as the current from transformer TR is being absorbed by inductor Lm. Nevertheless, switch S1 continues to conduct.

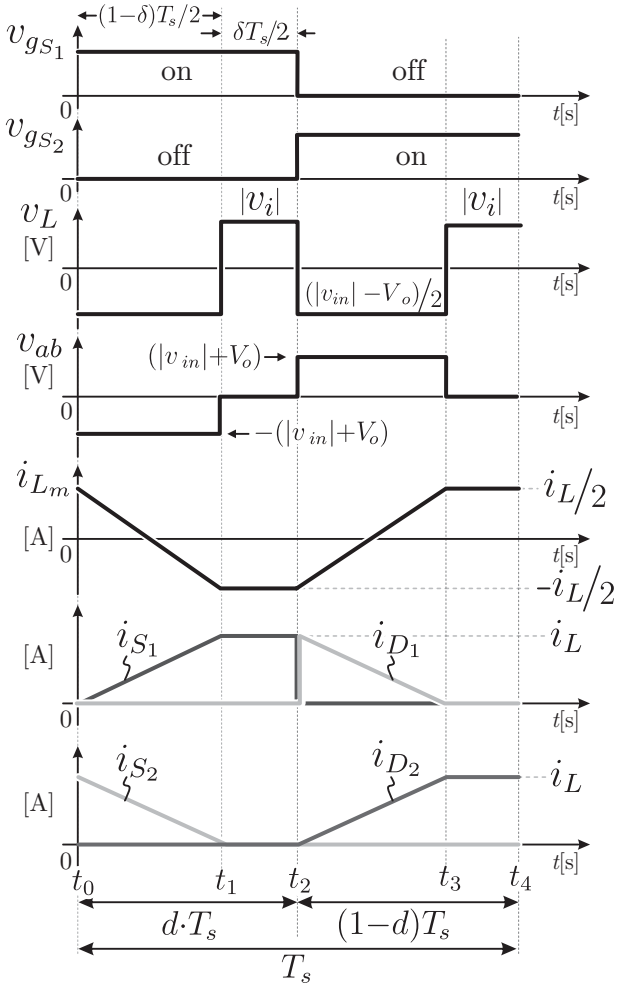


Figure 6 – Main wave forms

As there is no voltage over the inductor L_m, the voltage over the inductor L is [1], making so that it stores energy.

The voltage over the switches and diodes is the sum of the input voltage V_i and the output voltage V_o, as the studied converter is a rectifier, the maximum voltage over this forms components is obtained when the input voltage is at its peak. The conduction of the switches happens when there is a reversion on the voltage of the inductor L_m, making so that there is no current or voltage over the switch on its commutation being so a commutation with zero current and zero voltage transition (ZCZVT). When the current flows again due to the potential difference on the inductor L_m, the diodes start conducting and the switches commutation is with zero voltage transition (ZVT). This commutation processes present very small losses, due to that they dispense the need of auxiliary circuits and show promising results in efficiency.

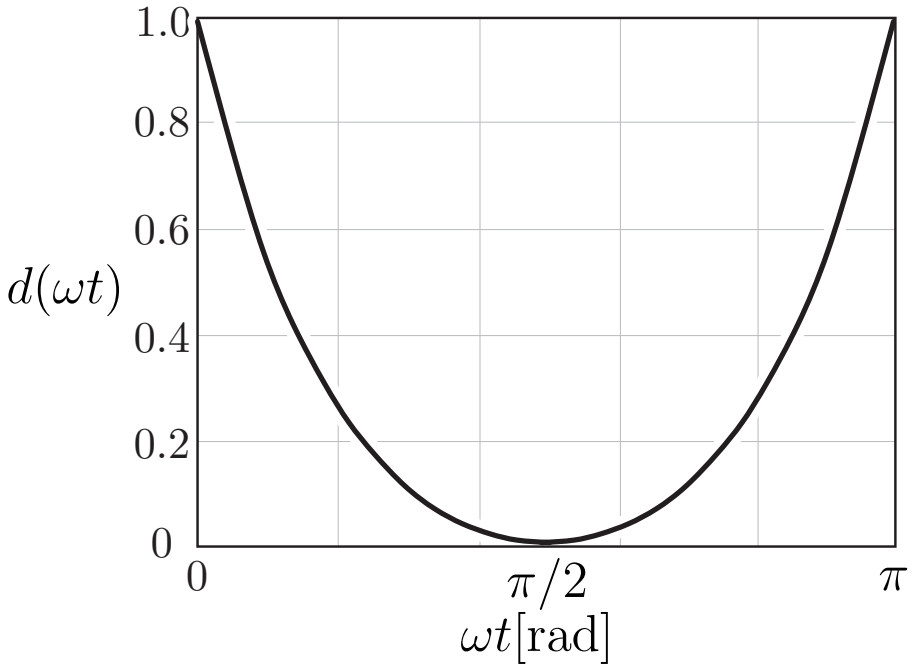
In order of obtaining the effective duty cycle it was necessary analyzing the average voltage over V_L (1) at steady state. After that analysis, the equation (7) is found, by isolating the effective duty cycle. The effective duty cycle behaviour during a line cycle can be seen on Fig. 7, this behaviour was obtained considering that the load and it's voltage remains the same throughout the hole cycle. The variable α is defined as V_p/V_o.

$$\delta(\omega t) = \frac{V_o - V_p \cdot \sin(\omega t)}{V_o + V_p \cdot \sin(\omega t)} \tag{5}$$

$$\overline{\delta}(\omega t) = \frac{\delta(\omega t)}{V_o} \tag{6}$$

$$\overline{\delta}(\omega t) = \frac{1 - \alpha \cdot \sin(\omega t)}{1 + \alpha \cdot \sin(\omega t)} \tag{7}$$

Figure 7 – Effective duty cycle



Source: Author

The current I_L is obtained by analysing the voltage over the inductance at V_L in $t = T_s/2$, different variations of I_L are presented in Fig. 9 .

$$I_L = ta \cdot \frac{V_p \cdot \sin(\omega t) + V_o}{L_m} \tag{8}$$

$$I_L = \frac{V_p \cdot \sin(\omega t)}{L_m \cdot fs} \tag{9}$$

The current of inductor L, as seen in (Hsieh; Hsueh; Yen, 2009), depends on the input voltage V_i, the magnetizing inductance and the switching frequency. For converters that behave as voltage followers as the ones mentioned before (Cuk (Simonetti; Sebastian; Uceda, 1997), Boost (Soares; Badin, 2021) and SEPIC (Simonetti; Sebastian; Uceda, 1997)), the output power of the converter can be controlled by the switching frequency.

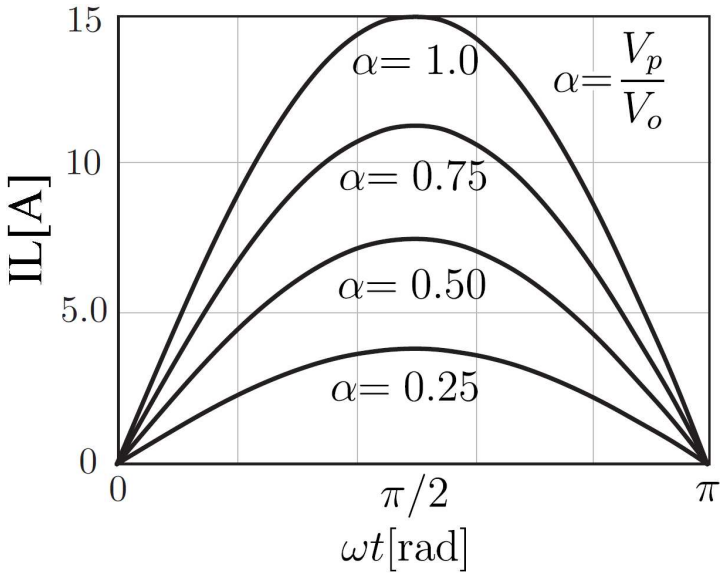


Figure 8 – Current I_L the inductor L in different variations of α.

2.4 Current Zero Crossing Distortion

$$T_{iL} = \frac{2 \cdot C_s \cdot V_o}{I_L} \tag{10}$$

When the diodes D_1 or D_2 blocks, another transition interval happens. This transition occurs between steps 2 and 3 and again between steps 4 and 1. In this transition the energy stored in the intrinsic capacitance of the switch and the diode of the arm which is momentarily parallel with the L_m inductor is transferred to the inductor and a freewheeling current "I_{fw}" is created to close the loop between switch and diode, this can be freewheeling current causes a Current Zero Crossing Distortion passage, providing harmonic distortion and changes in the PF. The intrinsic capacitances are directly proportional to the duration of both transition times as the equations bellow present. The transitional periods, that come com the freewheeling current, that impact the switching period are defined in [10] and [11].

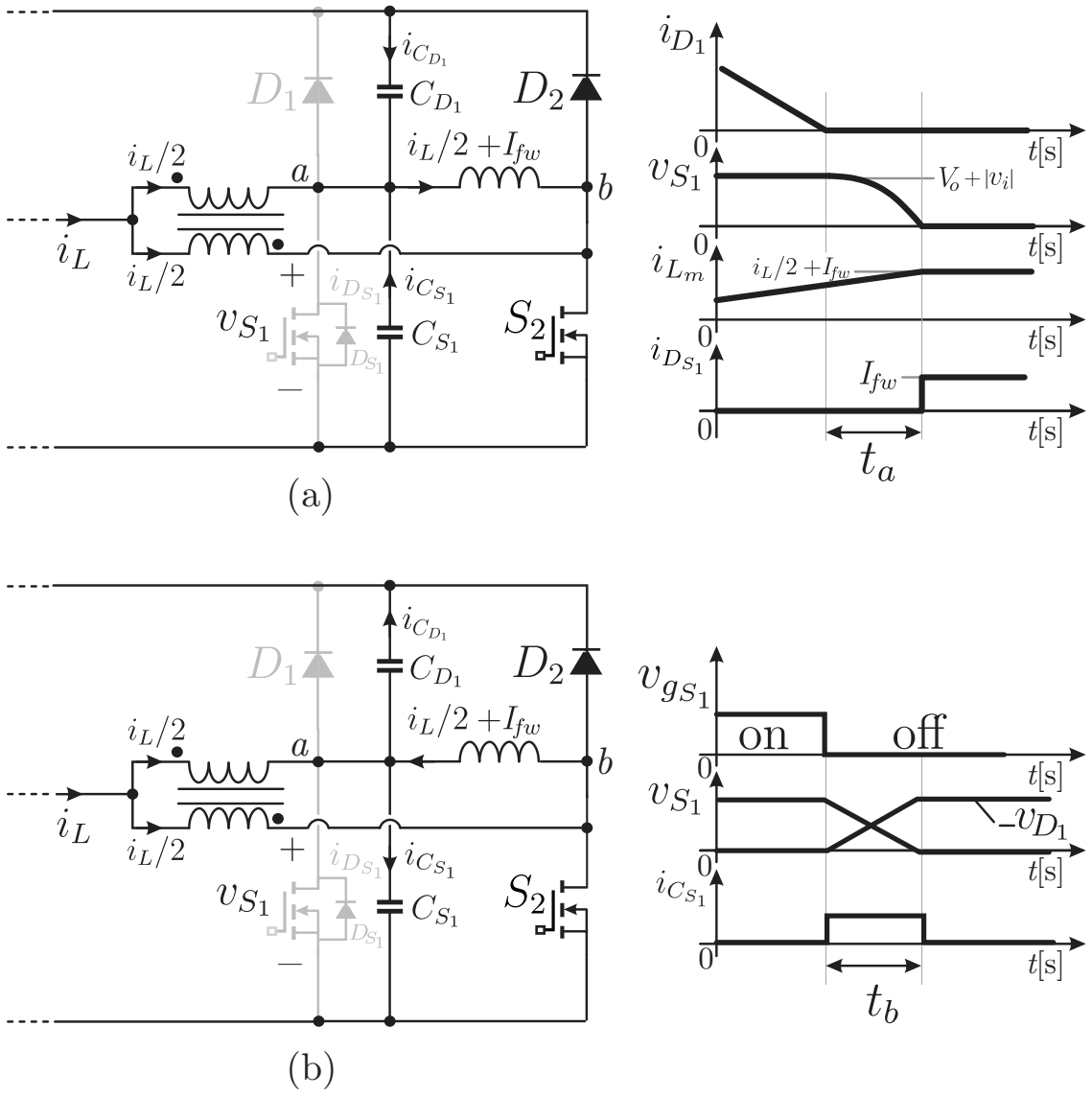
$$T_{I_2} = \pi \cdot \sqrt{2.L_m.C_s} \tag{11}$$

$$I_{fw} = V_o + V_{ret}(\frac{\pi}{2}) \cdot \sqrt{\frac{2 \cdot C_s}{L_m}} \tag{12}$$

$$ta = (\frac{\pi}{2}) \cdot \sqrt{2 \cdot C_s \cdot L_m} \tag{13}$$

By consideration the freewheeling current, the transition times in the I_L equation and the effective period equation(f_e being effective frequency, where "T"is the switching period) we have:

Figure 9 – Fig. a represents the commutation time interval when switch S1 turns off and diode D1 conducts, Fig. b represents the commutation time interval when diode D1 blocks.



Source: Author

$$f_e = \frac{1}{T - 2T_{iL} - 2T_{I2}} \tag{14}$$

$$I_L = \frac{V_p}{2 \cdot L_m \cdot f_e} - I_{fw} \tag{15}$$

The input current is defined by the equation [18] shows that the CCM buck-boost using PFM is not a perfect voltage follower, due to the input current being affected by the output voltage.

The frequency variation on the switches is defined in 17 by using the input current peak as its basis [16]. By applying the the conditions presented in [20] the article is able to show the interaction bet wen I_{fw} [12] and the input current. Fig. [10] presents a accurate simulation of the input current behaviour.

$$I_{pk} = \frac{2 \cdot P_o}{V_p} \tag{16}$$

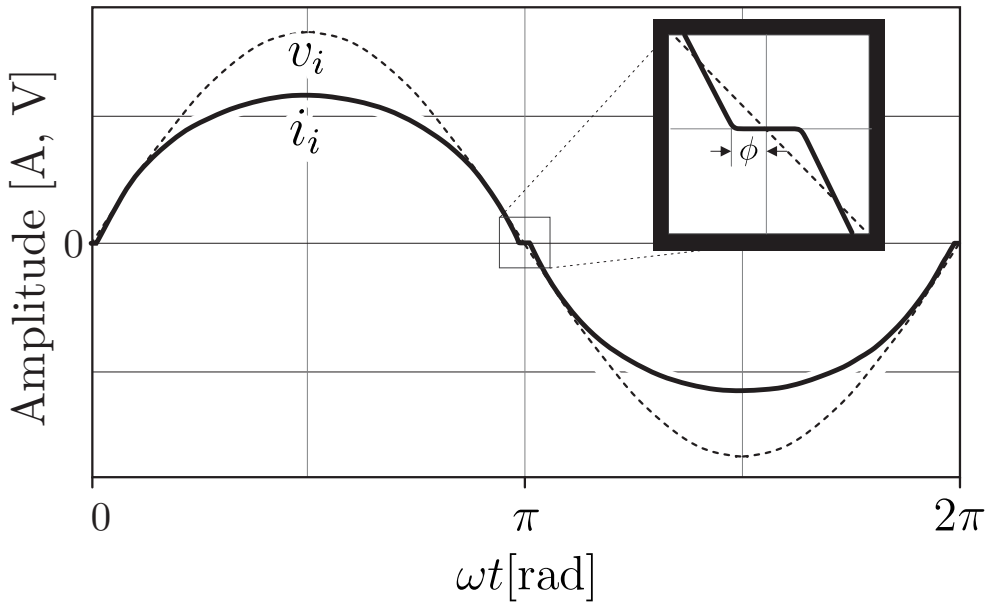
$$f_s = \frac{V_p}{P_o \cdot \pi} \cdot \int_0^{\pi} \frac{V_p \cdot \sin(\omega t)}{L_m} \left(\frac{V_o}{2(V_o + Vi \cdot \sin(\omega t)} \right) d\omega t \tag{17}$$

$$I_{in}(\omega t) = \frac{V_p \cdot \sin(\omega t)}{L_m \cdot fs} \cdot \left(\frac{V_o}{V_o + V_p \cdot \sin(\omega t)} \right) \tag{18}$$

$$\phi = (I_{fw}/I_{pk}) \tag{19}$$

$$I_{in}(\omega t) = \begin{pmatrix} 0A \;\; if \;\; 0 < \omega t \leq \phi \\ I_{pk}(\omega t) - Id \;\; if \;\; \phi < \omega t \leq (\pi - \phi) \\ 0A \;\; if \;\; \pi - \phi < \omega t \leq 2.\pi - \phi \\ I_{pk}(\omega t) + Id \;\; if \;\; \pi + \phi < \omega t \leq 2.(\pi - \phi) \\ 0A \;\; if \;\; 2.\pi - \phi < \omega t \leq 2.\pi \\ \end{pmatrix} \tag{20}$$

Figure 10 – theoretical input current.



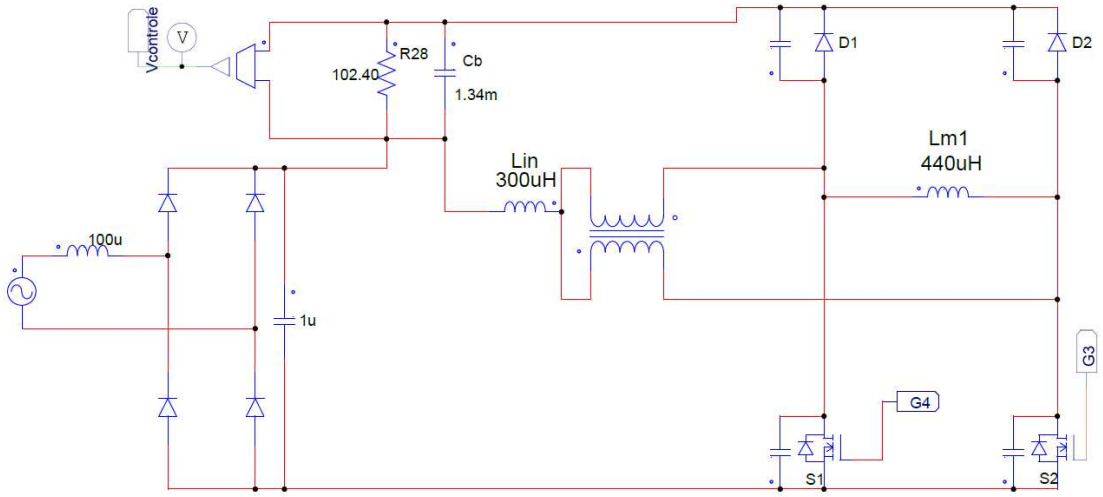
Source: Author

Considering the effective input current defined in [18] and its harmonic components, a study of the theoretical harmonic components of the converter was made and is presented on the section V Experimental Results.

3 PROPOSED CONVERTER SIMULATION

In order of proving the defined equations a simulation was made following the conditions of table 1, the simulation was made on the software PSIM. This simulation proves and provides the characteristics of the studied buck-boost converter, in both power and control. Figure 11 shows the simulated converter, and Fig. 12 shows the closed loop control utilized in the simulation. The high frequency figures were made analysing a input peak voltage of 225V. The most relevant results are presented in the following figures: Fig. 13 shows the medium and effective current over the switches; the Fig. 14 shows the voltage over the switches; the Fig. 15 shows the medium and effective current over the diodes; the Fig. 16 shows the voltage over the diodes; the Fig. 17 shows the current over the rectifying diodes. As for confirming the output voltage and its relation to the input current, figures 18 and 19 are presented. The input current THD is seen in 20.

Figure 11 – Simulated circuit.

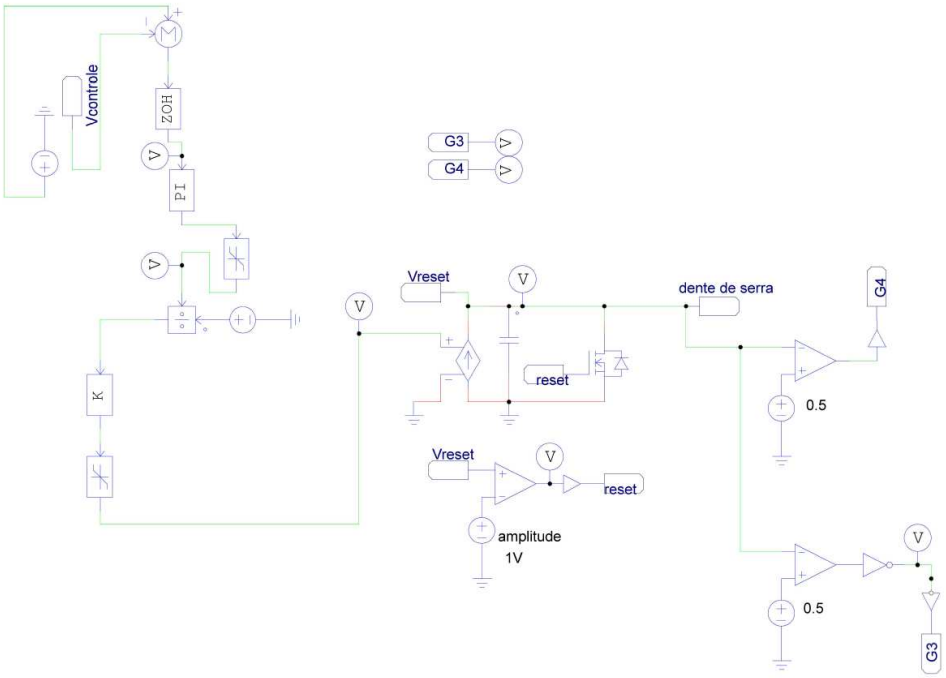


Source: Author

Table 1 – Simulation Parameters.

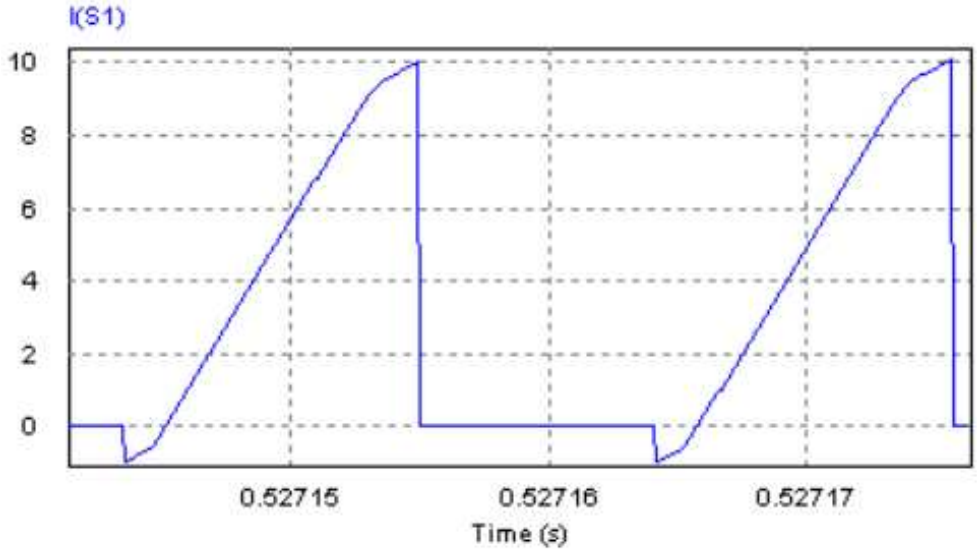
Parameter	Value
Output Power	P_o = 1000 W
Input Voltage	V_p = 311 Vpk
Output Voltage	V_o = 320 V
Inductance L	L = 300 μH
Auto Transformer	L_m = 110 μH
Output Capacitor	C_o = 1.34 mF

Figure 12 – Simulated input voltage and output voltage.



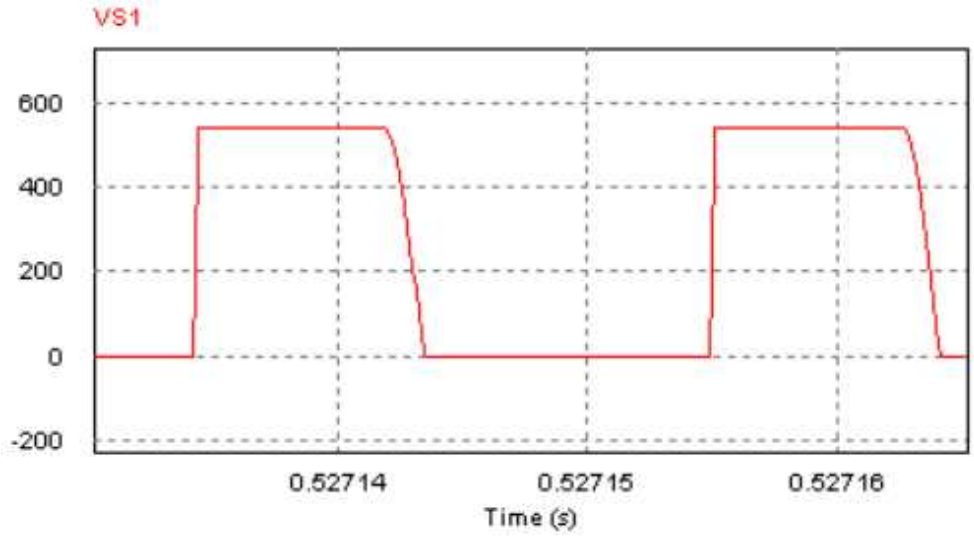
Source: Author

Figure 13 – Simulated switch current.



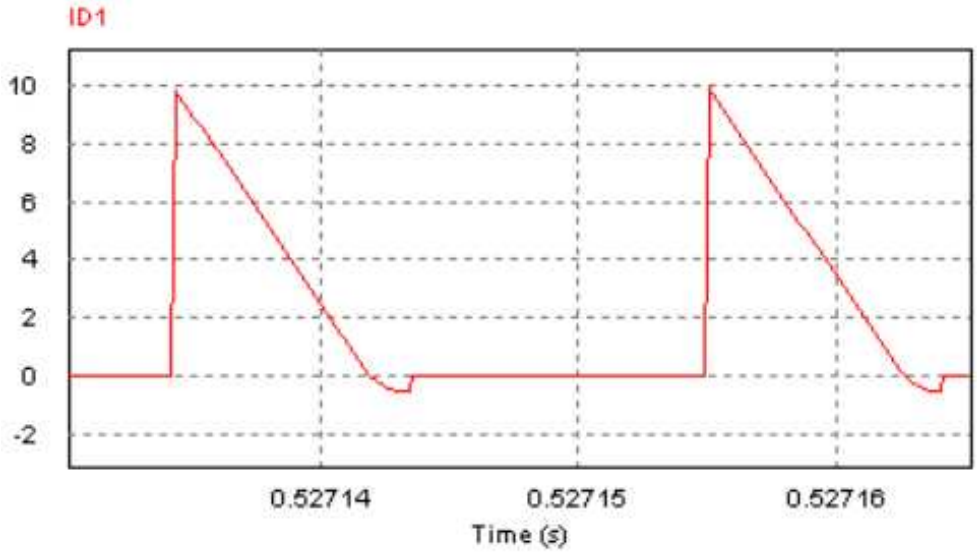
Source: Author

Figure 14 – Simulated switch voltage.



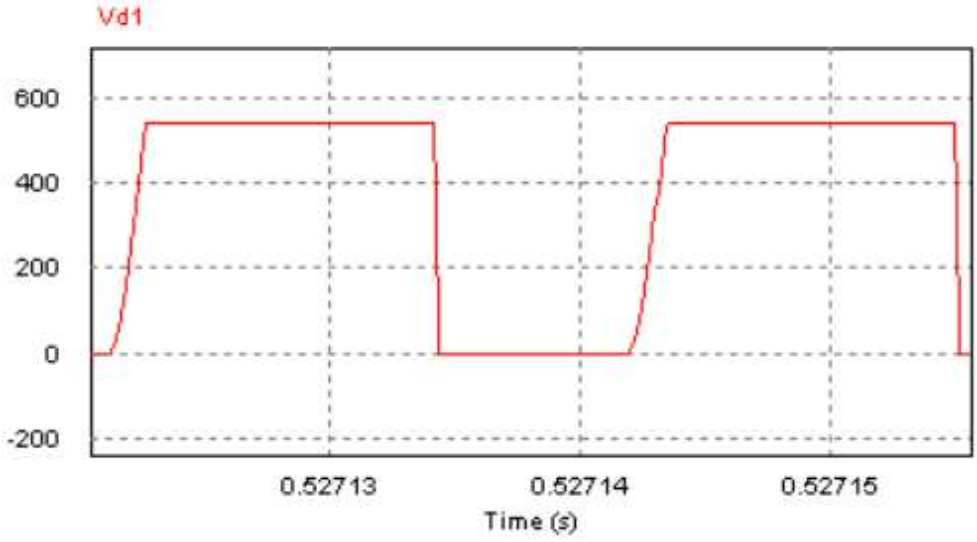
Source: Author

Figure 15 – Simulated diode current.



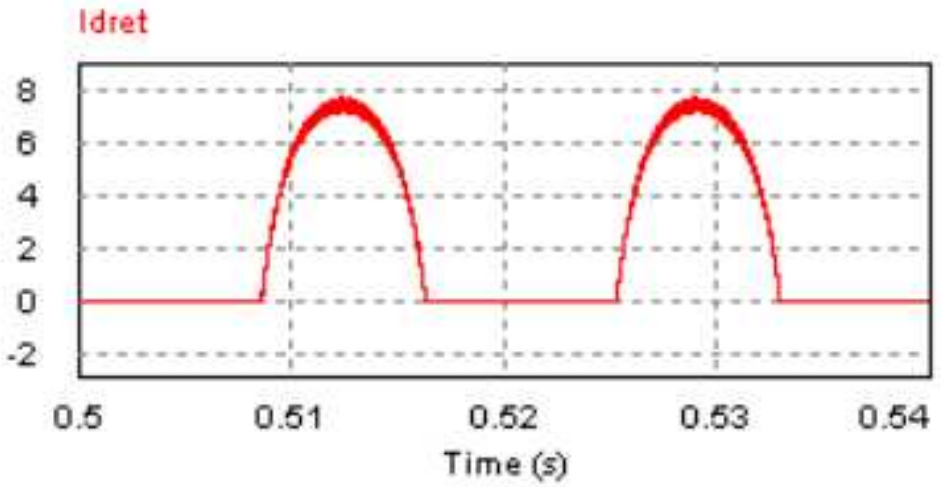
Source: Author

Figure 16 – Simulated diode voltage.



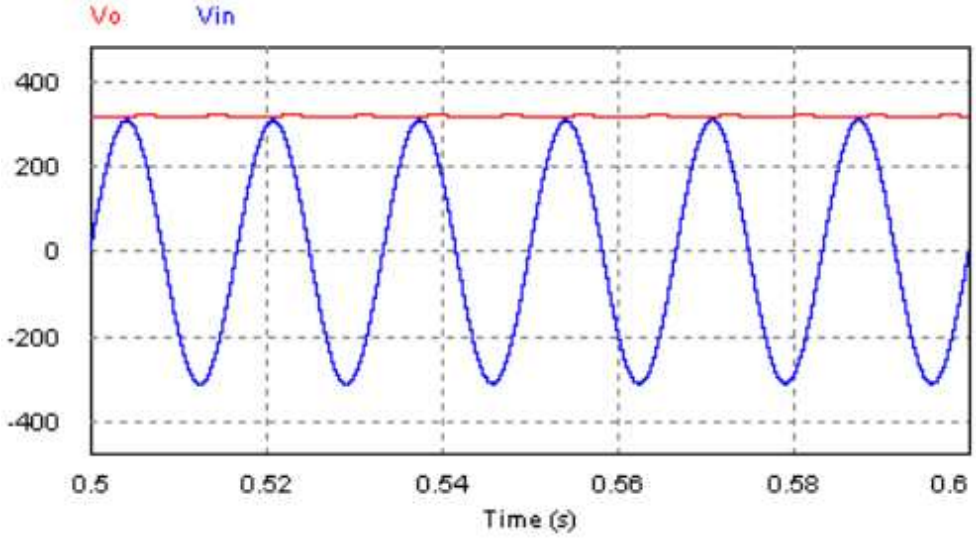
Source: Author

Figure 17 – Simulated rectifying diode current.



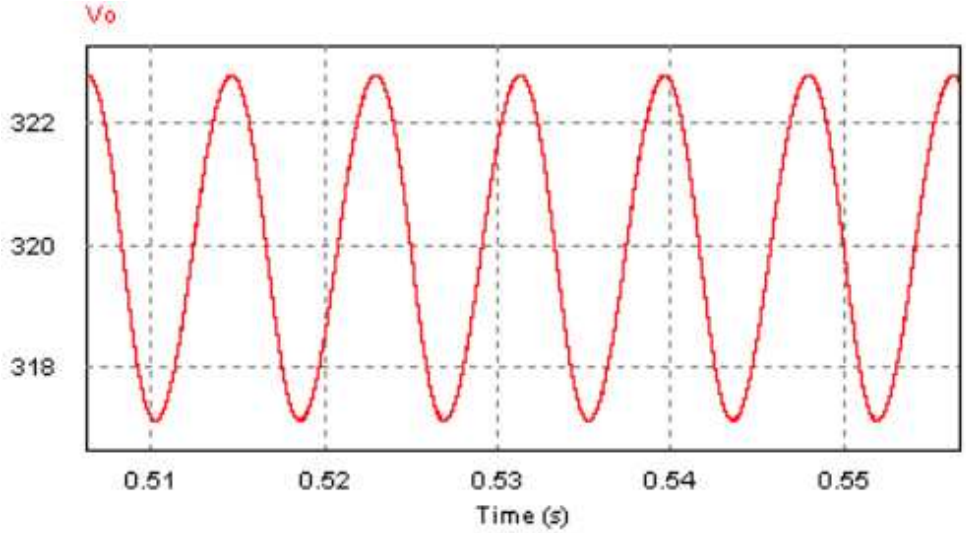
Source: Author

Figure 18 – Simulated input voltage and output voltage.



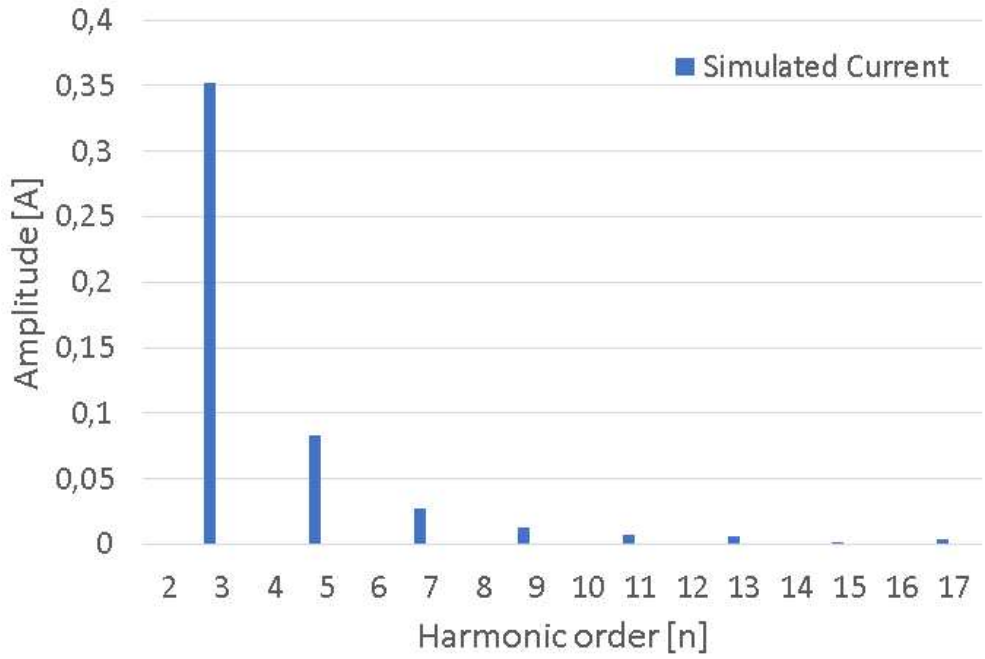
Source: Author

Figure 19 – Simulated output voltage.



Source: Author

Figure 20 – Simulated input current harmonic analysis.



Source: Author

4 LOSS ANALYSIS

The losses over the components are determined by the equations bellow, starting with the medium and effective switching current. The medium currents are represented by [21] that changes over time and [22] that is the medium current on the switches. The effective currents are represented by [23] that changes over time and [24] that is the effective current on the switches. The switching voltage is represented by [25], following by the diodes medium and effective current, and diodes voltage. The medium currents on the diodes are represented by [26] that changes over time and [27] that is the medium current on the diodes. The effective currents are represented by [28] that changes over time and [29] that is the effective current on the diodes. The voltage on the diodes are presented in [30] . All the presented equations were confirmed by the simulation results and its values are discussed in the experimental results, the wave format of the current and voltage on the semiconductors are presented both the proposed converted simulation, as the simulated results, and in the experimental results as the collected data from the converter prototype.

$$I_{smed}(\omega t) = \frac{I_L(\omega t) \cdot (1 - \delta(\omega t))}{4} + \frac{I_L(\omega t) \cdot \delta(\omega t)}{2} \tag{21}$$

$$I_{smed} = \frac{1}{\pi} \cdot \int_0^{\pi} I_{smed}(\omega t) d\omega t \tag{22}$$

$$I_{seff}(\omega t) = \sqrt{\frac{1}{T} \cdot \int_0^{t_a(\omega t)} \frac{(t \cdot (v_o + v_i))^2}{L_m^2} d\omega t + \int_{t_a(\omega t)}^{\frac{T}{2}} I_L(\omega t)^2} \tag{23}$$

$$I_{seff} = \frac{1}{\pi} \cdot \int_0^{\pi} I_{seff}(\omega t) d\omega t \tag{24}$$

$$V_s = Vi + Vo \tag{25}$$

$$I_{dmed}(\omega t) = \frac{I_L(\omega t) \cdot (1 - \delta(\omega t))}{4} \tag{26}$$

$$I_{dmed} = \frac{1}{\pi} \cdot \int_0^{\pi} I_{dmed}(\omega t) d\omega t \tag{27}$$

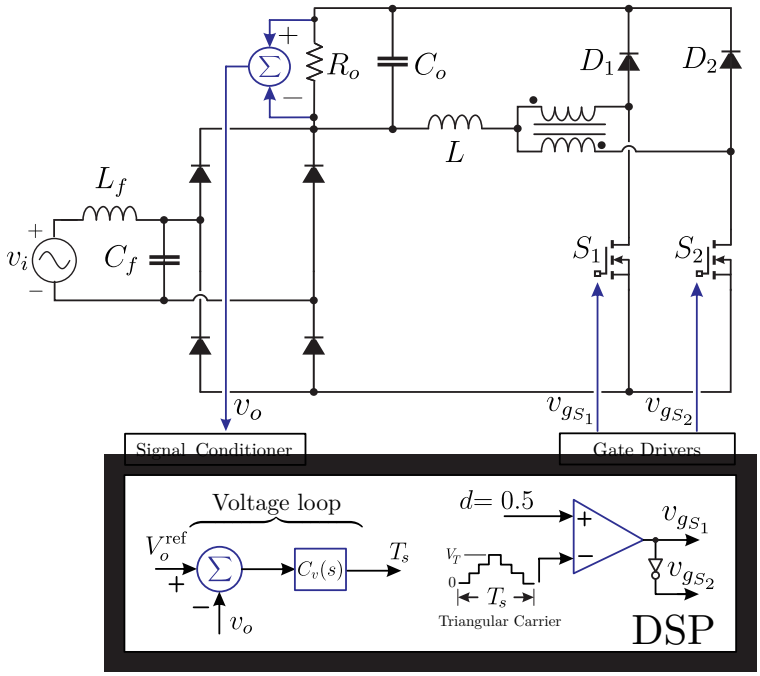
$$I_{deff}(\omega t) = \sqrt{\frac{1}{T} \cdot \int_0^{t_a(\omega t)} \frac{(t \cdot (v_o + v_i))^2}{L_m^2} d\omega t} \tag{28}$$

$$I_{deff} = \frac{1}{\pi} \cdot \int_0^{\pi} I_{deff}(\omega t) d\omega t \tag{29}$$

$$V_d = Vi + Vo \tag{30}$$

5 CONTROL STRATEGY

Figure 21 – Detailed control scheme.



Source: Author

The usual buck-boost CCM converters need a current loop in order to stabilize it's control (RESTREPO *et al.*, 2019), (LEE *et al.*, 2012), (RESTREPO *et al.*, 2012),(CHUB *et al.*, 2017),(RAMíREZ-MURILLO *et al.*, 2014). As mentioned in the previous sections, the converter proposed in this paper is a voltage follower due to the PFM control, so the input power will change according to the frequency of the modulation, so a current feedback loop is not needed. This brings out several advantages to the converter that can reduce its cost and complexity such as as:

- Simplifying its construction and control.
- Reducing the need of a powerful and expansive DSP.
- Making so that hall sensors are not needed for the control.

Although the DPS would not need to be powerful, the used DSP on the prototype is very powerful, it was opted to use this DPS due to it's availability on the laboratory and it's already known uses.

In order to control the modulation an output voltage feedback loop was settled, Fig. 21 presents the control scheme, where the output voltage V_o is the feedback of the PI controller, the result provides the switching period Ts, than the DSP changes the switching frequency and

applies a command to the drivers, theses will feed the gate of the switches with a fixed duty cycle of 0.5 and a 180º phase shift.

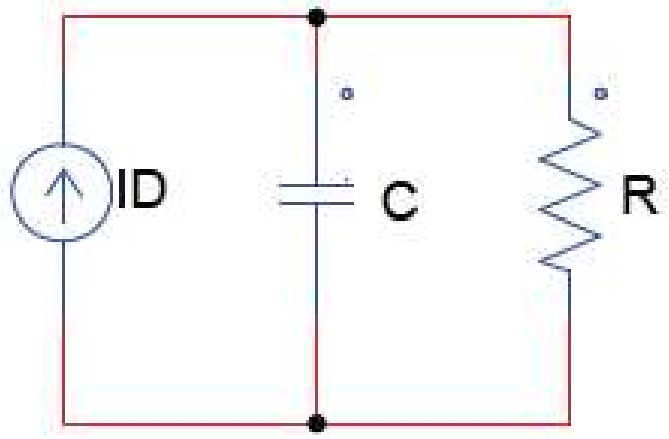
For obtaining the PI controller parameters a linearized model of the converter's plant is made. This model is based on the principle of energy distribution across the passive components of the converter [31].

$$i_o(t) = i_C(t) + i_R(t) \tag{31}$$

This equation do not consider the the energy on the auto-transformer, filter inductor and on the components intrinsic capacitances. Nevertheless the dynamic model of the converter is obtained in this equation on a satisfactory way, considering just the energy on the output capacitor and the resistance.

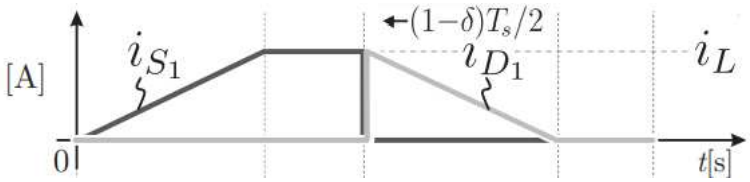
On the equation [31], $i_o(T)$ the output current, $i_C(T)$ the current accumulated on the output capacitor and $i_R(T)$ the current received by the converters load. By analysing the current nodes of the simplified circuit of the converter 22, and considering the output current equals to the diodes current [27], that it is described by fig 23 and the equation [32]. In this equation the terms v_o represents the output Voltage and F_s represents the switching frequency.

Figure 22 – Simplified output current circuit.



Source: Author

Figure 23 – Diode current.



Source: Author

$$i_o = i_d = \frac{I_L \cdot (1-\alpha)}{2} = \frac{v_p^2}{8 \cdot L_m \cdot F_s \cdot v_o} \tag{32}$$

The current on the output capacitor $i_C(T)$ is presented in 33 and the power received by the converters load $i_R(T)$ is presented in 34, where R is the load resistance, and C the output capacitance.

$$i_C = \frac{dv_o(t)}{dt} \tag{33}$$

$$i_R = \frac{v_o(t)}{C \cdot R} \tag{34}$$

Utilizing the now developed equations, the current distribution over the converter is re-written in 35

$$\frac{v_p^2}{8 \cdot L_m \cdot F_s \cdot v_o} = \frac{dv_o(t)}{dt} + \frac{v_o(t)}{C \cdot R} \tag{35}$$

In order of obtaining a simplified model of the converter if first necessary to apply the apply the Laplace transform on equation 35.

$$\frac{v_p^2}{8 \cdot L_m \cdot F_s \cdot v_o} = \frac{dv_o(t)}{dt} + \frac{v_o(t)}{C \cdot R} \tag{36}$$

After applying the Laplace transform in 36 equation 37 is obtained, this equation presents the power distribution on the frequency domain. Where T_s represents the switching period.

$$\frac{v_p^2 \cdot T_s(s)}{8 \cdot L_m \cdot F_s \cdot v_o \cdot C} = s \cdot v_o(s) + \frac{v_o(s)}{C \cdot R} \tag{37}$$

By simplifying equation 37 it is obtained the model of small signs of the voltage loop of the converter 38. $G_v(s)$ represents the transfer function of small signals that co-relates the variation in the output voltage and with the switching period.

$$G_v(s) = \frac{\tilde{v_o}(s)}{\tilde{T_s}(s)} = \frac{v_p^2 \cdot R}{8 \cdot L_m \cdot C \cdot v_o \cdot (R \cdot C \cdot s + 1)} \tag{38}$$

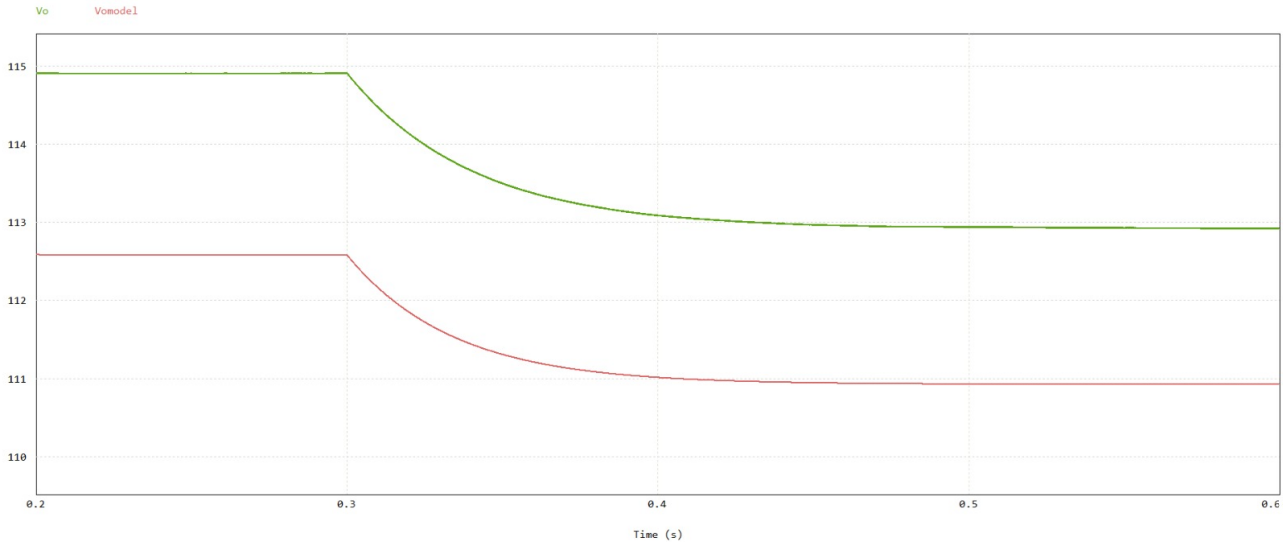
The transfer function is tested in a PSIM simulation and compared to the output voltage of the simulated converter, the result is presented in 24. This simulation shows a static error, but the dynamic response is accurate.

In order of testing the effectiveness of the PI controller a simulation was made on PSIM software, this simulation presents the conditions stated in table 2:

Fig. 26 represents the simulated result of a 50% load variation on the output current, demonstrating the effectiveness of the controlled system.

In addition a soft-starter command was programmed in the DSP, this command define that the duty cycle of the converter starts at 0, and grow every 5 millisecond until it reaches 0.5, this command guarantee that the converter can start with the full output power without stressing the control.

Figure 24 – Simulated transfer function.

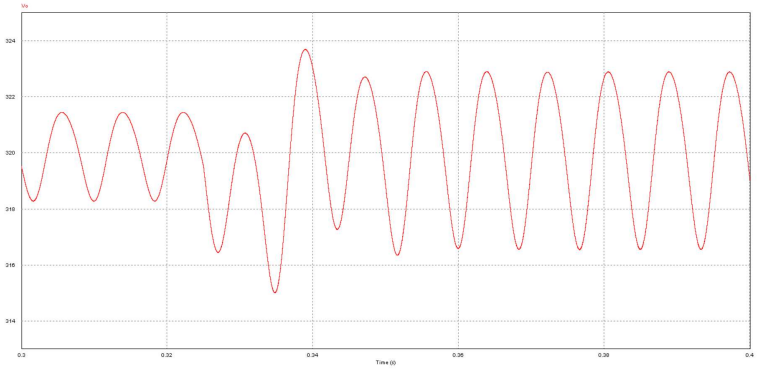


Source: Author

Table 2 – Simulation Parameters for the Control Test.

Parameter	Value
Output Power	P_o = 1000 W
Input Voltage	V_p = 311 Vpk
Output Voltage	V_o = 320 V
Inductance L	L = 300 μH
Auto Transformer	L_m = 110 μH
Output Capacitor	C_o = 1.34 mF

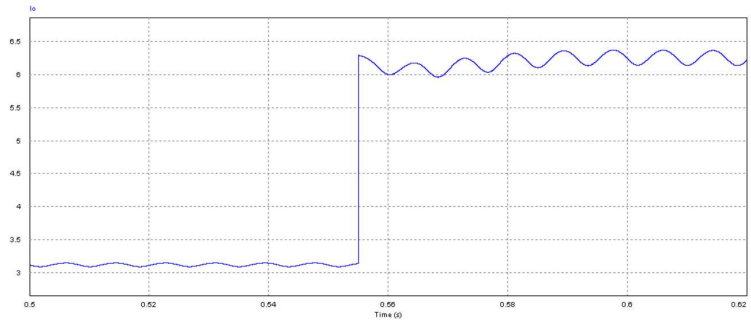
Figure 25 – Simulated control 50% load variation (Output Voltage).



Source: Author

The fig. 40 represents the control loop code that was wrote in order of stabilizing the output power, for the loop was used the control basis analysis. On this matter is crucial to understand that the system should be sustained in the long term by the integer (Integral) and should only be accelerated by the proportional (proporcional).The control loop is also based on the period for a better result, nevertheless it could be based in the frequency for obtaining similar results. The complete code is also presented in Apendix A.

Figure 26 – Simulated control 50% load variation (Output Current).

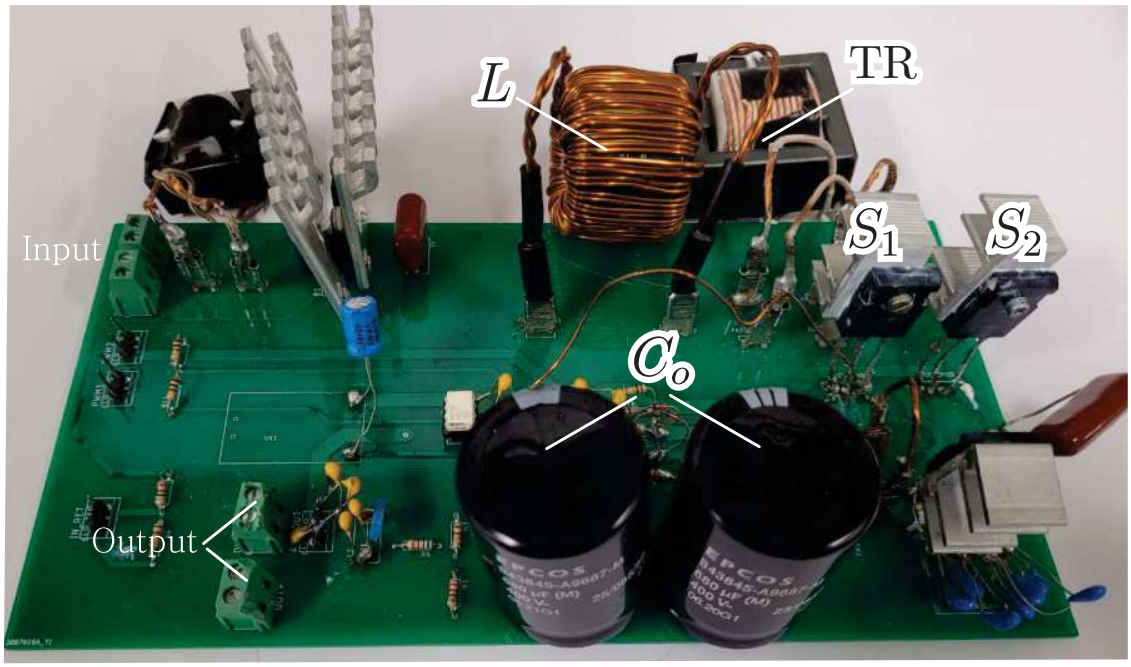


Source: Author

6 EXPERIMENTAL RESULTS

In order of testing the presented converter a prototype was made, Fig. 27 presents the prototype of the converter. The converter layout was made using the software eagle and was optimized for taking measurements in order of testing it. Fig. 28 shows its circuit board layout. On the circuit board the main components are: The filter inductor, the diode bridge, the filter capacitor, the auto-transformer, the switches, the power diodes (both in one package) and the output capacitors. As for the control there is a 15V power source, there are 2 drivers (one for each switch) that need a circuit of resistors and capacitors for its perfect function, finally there is a resistor divisor for the control loop, which is connected to the DSP F28379D.

Figure 27 – Converter prototype.



Source: Author

To build the inductors and transformer as needed for the prototype, the following equations were used:

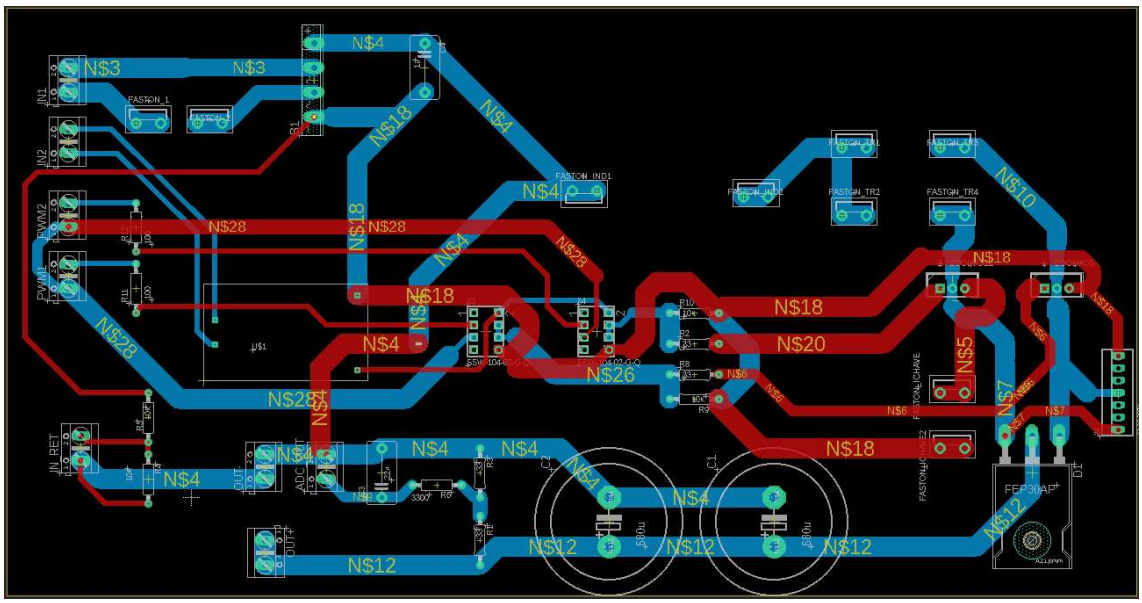
$$AeAw = \frac{L \cdot IL_{pk} \cdot IL_{ef}}{B_{max} \cdot K_w \cdot J_{max} \cdot 10^{-4}} \tag{39}$$

$$N = \frac{L \cdot IL_{pk}}{B_{max} \cdot A_e \cdot 10^{-4}} \tag{40}$$

$$Space = \frac{N \cdot Wire_{section}}{Kw \cdot Aw} \tag{41}$$

Equation 39 is used in order of defining the most suited core for the inductor or transformer, equation 40 is used in order of calculating the number of coil turns that will be needed. At

Figure 28 – circuit board layout



Source: Author

last equation 41 is used in order of checking if there is space for the number of coils calculated, if space is smaller than one than the construction is viable. The Kw variable is usually 0.7, and it represents a coefficient that helps correcting the errors of building a inductor or transformer by hand, guaranteeing that will be more space available than the equation would first show. For the studied converter the chosen nucleon for the filtering inductor was E-42/15, the number of coils was 32. For the auto transformer the chosen nucleon was E-30/14, the number of coils is 29 each side. The main inductor is store bought with 300uH.

This section present the results obtained with the constructed buck-boost converter applying the switching cell and the PFM. The parameters in which the converter was constructed are displayed on the Table 3.

For accomplishing the objective of analysing the wave formats resemblance of experimental and theoretical data, measurements were made beginning with the data found in Fig. 30. This figure shows the voltage over the switch (V_{s1}) the voltage over the diode (V_{d1}) and the current over the switch (I_{s1}), the voltage values are the same as described in Fig. 6 stating that the initial analysis was correct.

By analysing Fig. 30 it is possible to see that the current and the voltage over switch S_1 are both zero when the switch S_1 turns on, as stated before, the same can be considered to switch S_2, these commutations are partially zero current switching (ZCS) and are zero voltage switching (ZVS), which shows that the commutation losses are very low, improving the efficiency of the converter.

Fig. 31 shows the current in the inductor I_L in low frequency and high frequency, the wave format and its value are very similar to the ones presented in Fig. 9, also presenting two times the switching frequency in its high frequency analysis, which is an advantage of this topology, making so that the inductor L can be smaller and lighter.

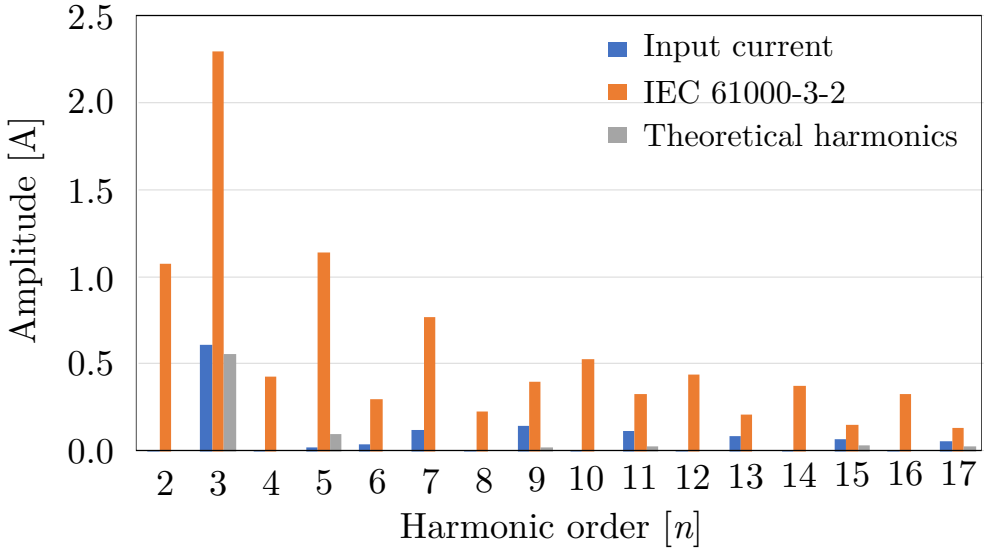
Fig. 32 show the output voltage, the current in the inductor L in low frequency and the voltage over the inductor L. This figure presents the low variation in the output voltage when analysing in high frequency and shows the current variation on the inductor that happens according to twice the switching frequency.

Fig. 33 represents the input voltage and input current, in that we can see that there is a small distortion on the current, making so that is not perfectly a sine function, as defined by equation 18. By analysing this wave format csv file in the PSIM simulator, we were able to find the total harmonic distortion (THD), that is defined as 10% and that its power factor is 0.994. Fig. 35 shows in more detail the instant when zero crossing distortion is present, this distortion is caused by the freewheeling current 12 over the inductor L.

Fig. 34 represents the controlled system after a 50% reduction in the output power. The system only takes a few grid cycles in order to stabilize, showing the efficiency of its simple voltage control.

Fig. 29 shows the total harmonic distortion study made using the experimental data collected on the oscilloscope analysed using the PSIM software. In addition, the comparison between the theoretical calculation of the harmonics amplitude, the harmonic amplitude measured in the prototype and the standard reference from IEC 61000-3-2 are also presented in Fig. 29, this figure represents the different harmonic components between 2-17 times the input current frequency. By analysing Fig. 29 the conclusion obtained is that the THD in the converter and its prototype is within the normative values for every harmonic order analysed. The THD analysis together with the power factor values obtained shows a promising performance as a PFC.

Figure 29 – Total harmonic distortion on the input current represented in blue, IEC 61000-3-2 harmonic distortion limits represented in orange and theoretical harmonic distortion represented in grey.



Source: Author

Table 3 – Experiment Parameters.

Parameter	Value
Output Power	P_o = 1000 W
Input Voltage	V_p = 311 Vpk
Output Voltage	V_o = 320 V
Switch Frequency	f_s = 30 - 250 kHz
Inductance L	L = 300 μH
Auto Transformer	L_m = 110 μH
Output Capacitor	C_o = 1.34 mF
Filter Inductance	L = 100 μH
Filter Capacitance	C = 1 μF
Switches	SiC CREE C2M0025120
Switching Diodes	SiC
Rectifying Diodes	Ultra Fast
Drivers	FOD 3180
DSP	F28379D Texas Instruments

Table 4 – Data Analysis

data	Calculated	Simulated	Experienced
medium switch current	2.36A	2.13A	1.81A
effective switch current	4.05A	3.74A	3.28A
medium diode current	1.73A	1.55A	1.74A
effective diode current	3.41A	3.25A	3.44A

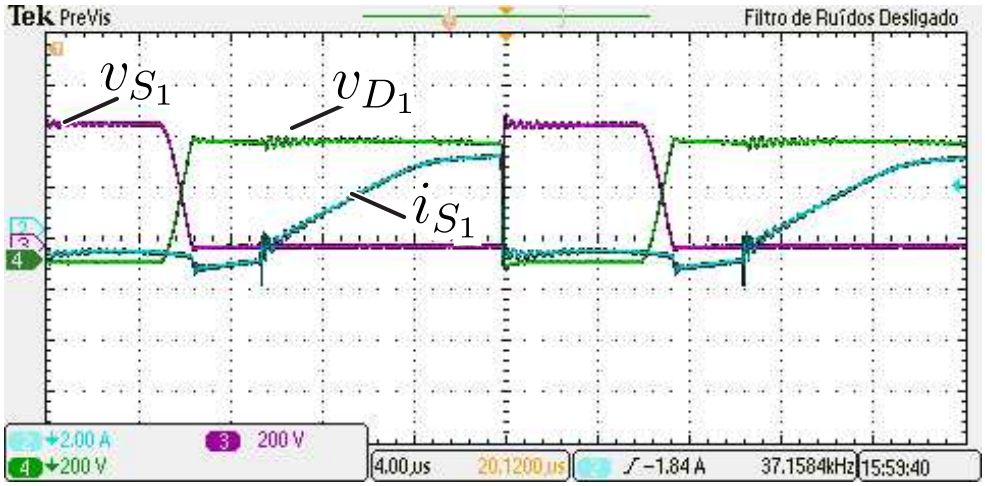
The acquired wave forms are shown in Fig. 30 to 33. They were acquired under the conditions stated on Table I. Fig. 30 shows the current and voltage over the switch and the voltage over the diode. Fig. 31 shows the current over the inductor L in low and high frequency. Fig. 32 shows the inductor voltage and current together with the output voltage. Fig 33 shows the passage over zero happening in the input current. Fig 36 presents the efficiency curve obtained through the tests.

In order to compare the differences between simulated data, theoretical analysis and experimental results, the table 4 shows the result of all 3 analysis for the same conditions as stated in table 3:

6.1 Double Modulation

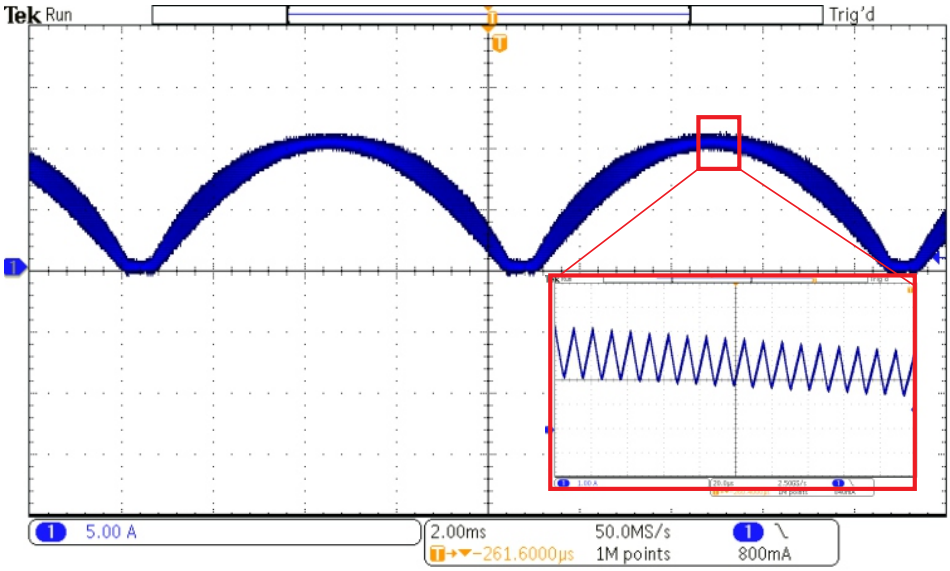
The operations shown so far have presented the converter working as a Boost converter, in order of operating it as a Buck a change in its modulation must be made, making so that a

Figure 30 – Switch voltage v_{s1} represented in violet, diode voltage v_{d1} represented in green, switch current i_{s1} represented in cian. Buck-boost experiment with the studied switching cell, CCM operation with 1 kW output and 47 kHz frequency



Source: Author

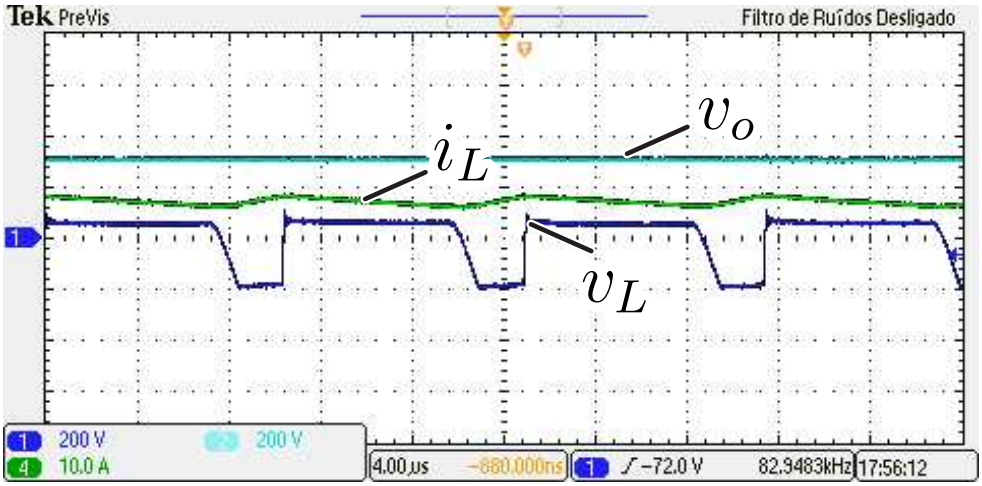
Figure 31 – Current over inductor L represented by i_L cian. Buck-boost experiment with the studied switching cell, CCM operation with 1 kW output and 47 kHz frequency



Source: Author

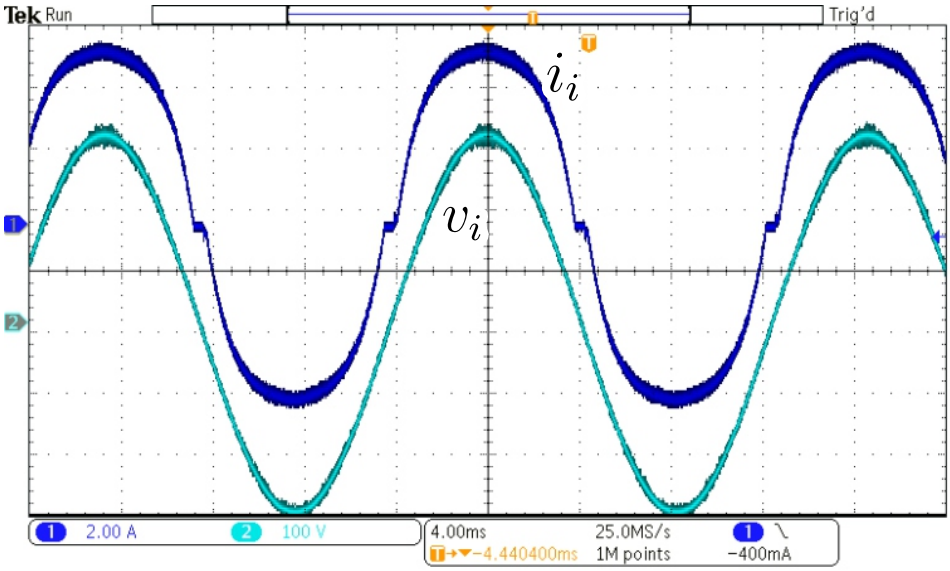
double modulation standard was now necessary, the modulation is now related to both , duty cycle and frequency. The previous current control mode, which worked by changing the frequency in order of controlling the output voltage is still the main form of controlling the converter output voltage, nevertheless the duty cycle that was maintained at 0.5 for the Boost operation needs to be reduced for controlling the output voltage at a lower level than the input voltage, presenting than the Buck operation.

Figure 32 – Voltage output represented by v_o cian, voltage over the inductor L represented by v_l blue. Current over inductor L represented by i_L green. Buck-boost experiment with the studied switching cell, CCM operation with 1 kW output and 47 kHz frequency



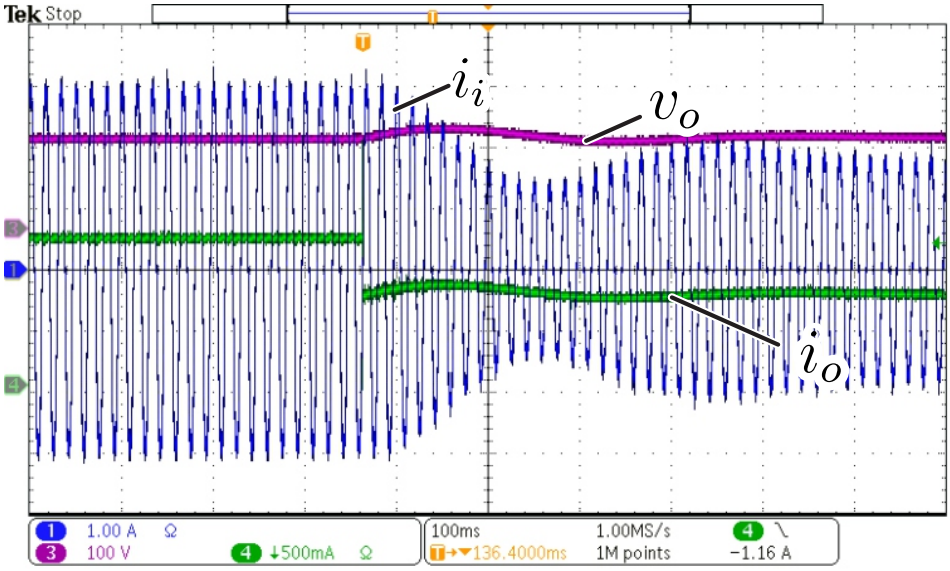
Source: Author

Figure 33 – Voltage input represented by v_i cian, current input represented by i_i green. Buck-boost experiment with the studied switching cell, CCM operation with 1 kW output and 47 kHz frequency



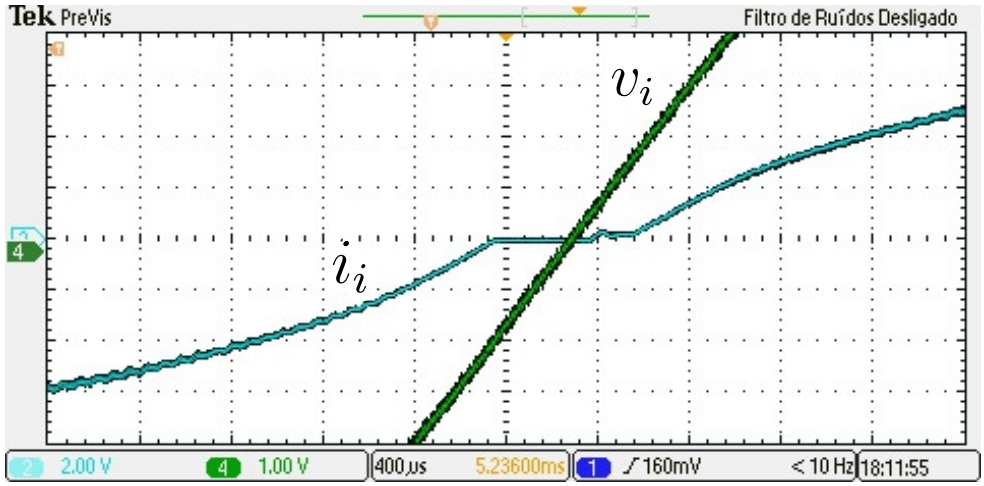
Source: Author

Figure 34 – Control response to output power change. Output voltage v_o represented in cian, output current represented in blue, input current represented in green.



Source: Author

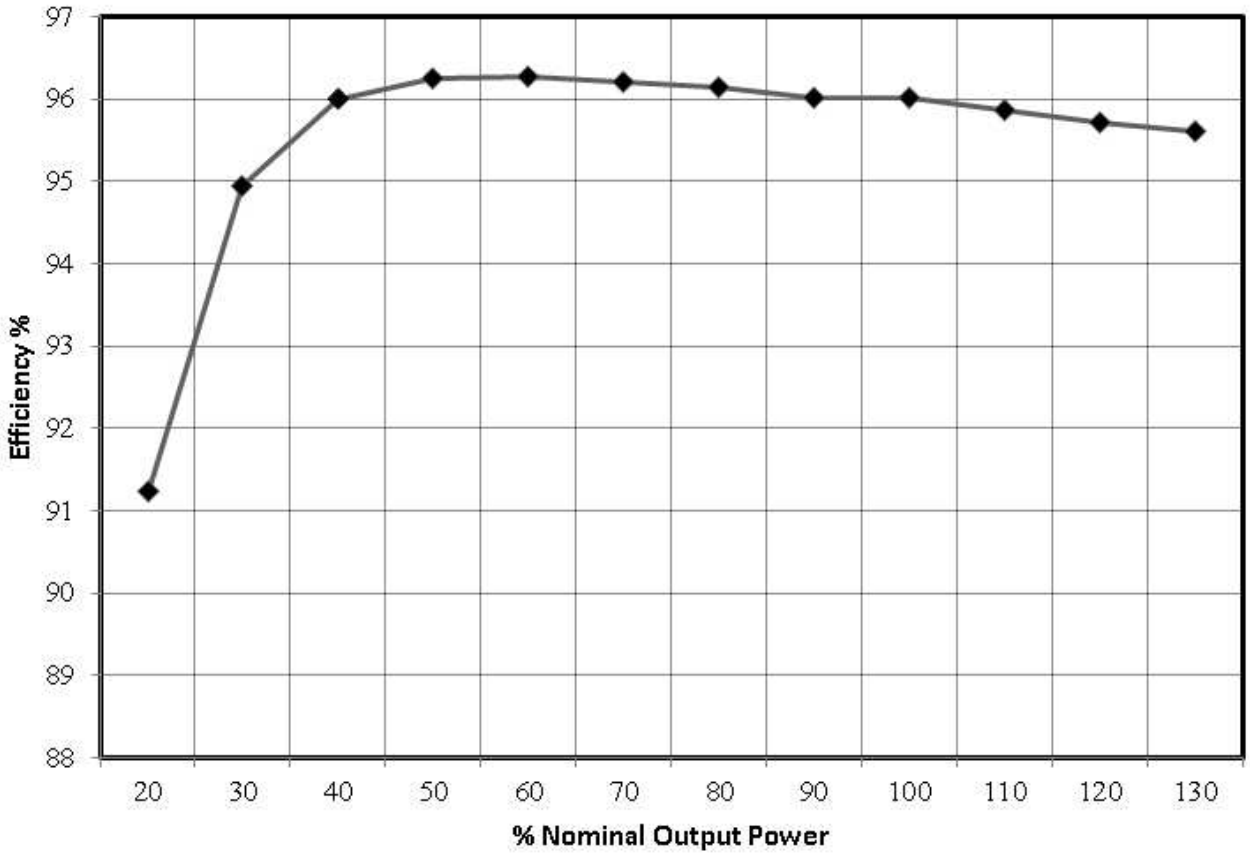
Figure 35 – Passage over zero. Voltage input represented by Vv$_i$ Green, current input represented by I_i Cian. Buck-Boost experiment with the studied switching cell, CCM operation with 1 kW output and 47 kHz frequency



Source: Author

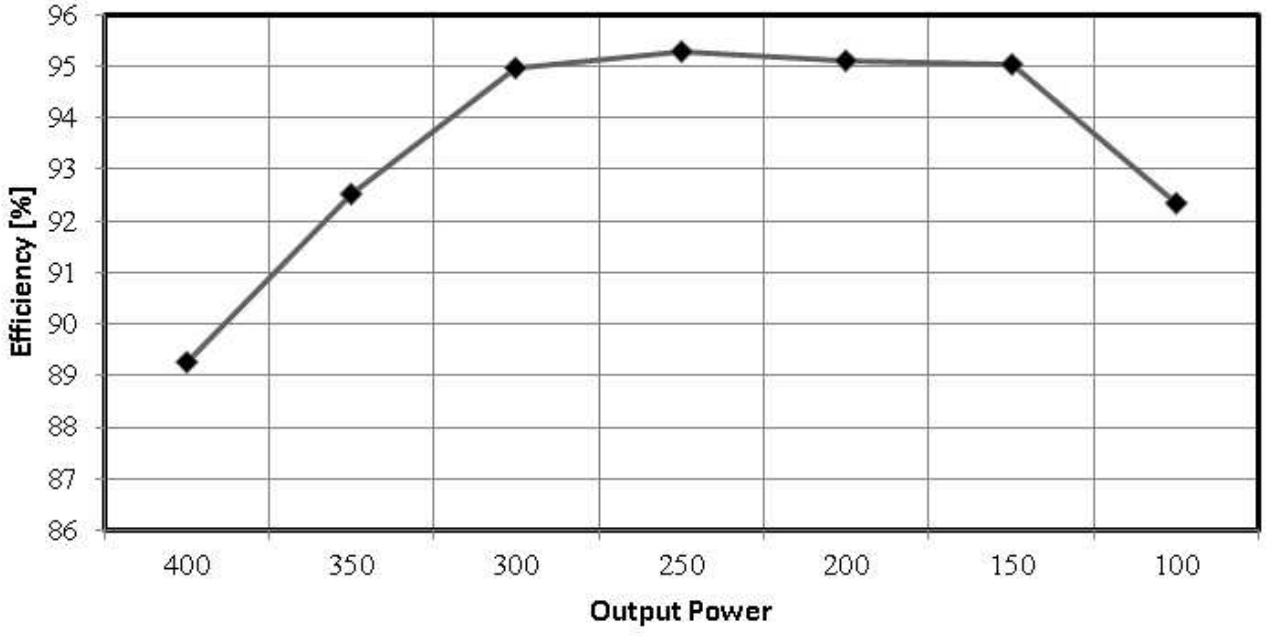
For testing this operation method a new set of parameter was defined and is presented at the table 5. In this test the efficiency of the converter was measured in different output powers, the results can be seen in Fig. 37. The buck operation can be confirmed in Fig. 38, where the input voltage can be seen having a bigger output value than the input voltage, also the input current is shown and is presented as having a distortion, its harmonic analysis is presented in Fig. 39, and its THD is found to be 15

Figure 36 – Curve of efficiency of the converter in Boost mode



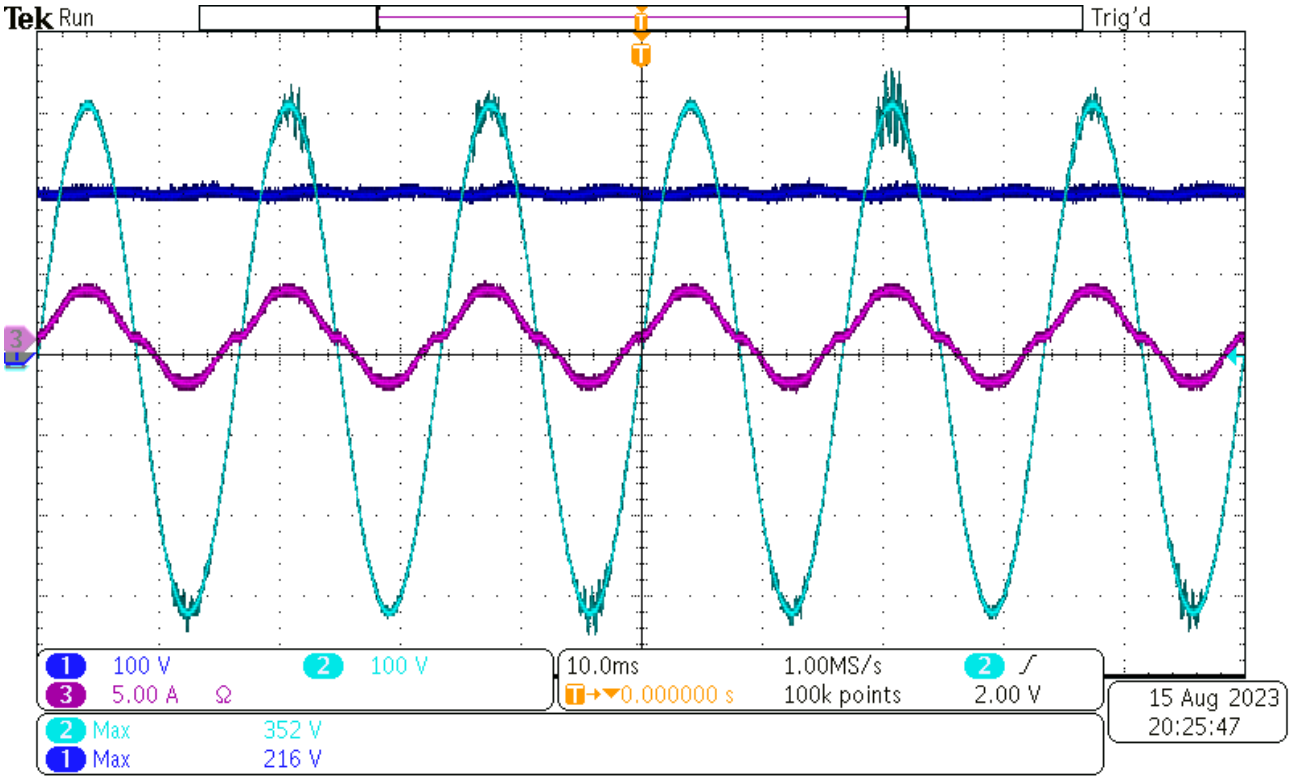
Source: Author

Figure 37 – Curve of efficiency of the converter in Buck mode



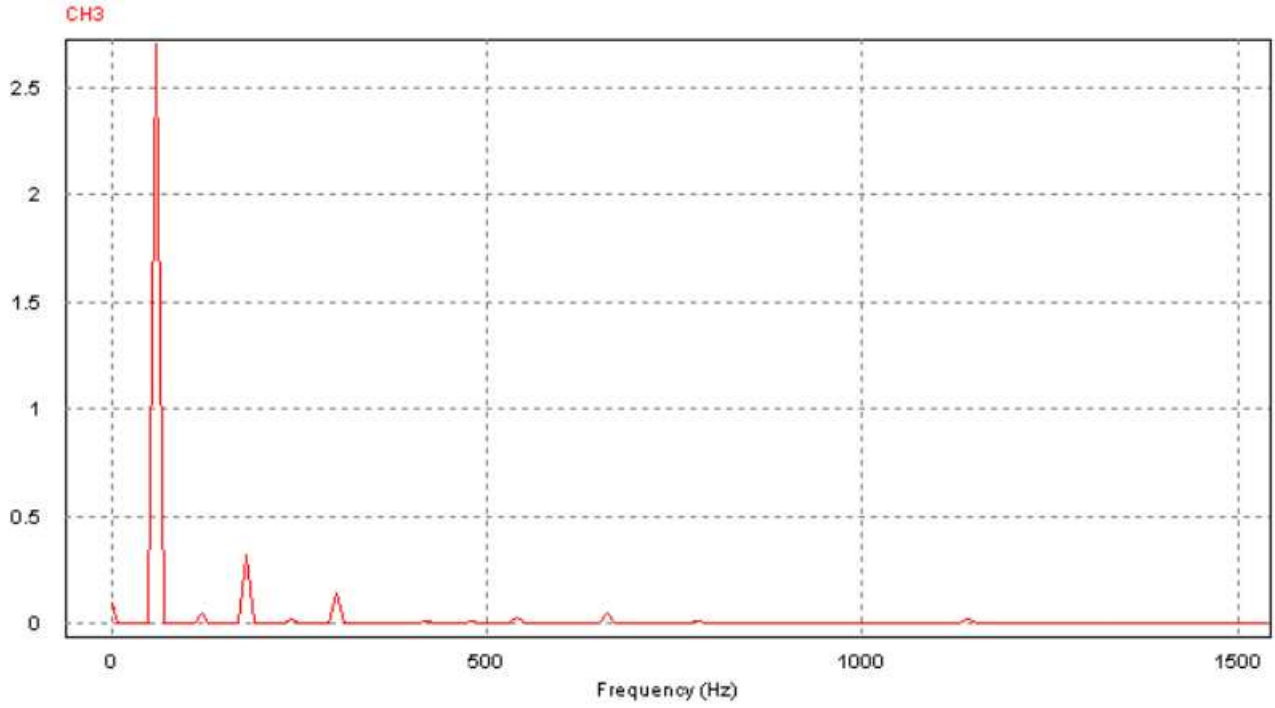
Source: Author

Figure 38 – Curve of efficiency of the converter in Buck mode, in Cian, input voltage vi is presented, in Blue, output voltage vo is presented, in Violet the input current is presented.



Source: Author

Figure 39 – Input current harmonic analysis, in buck mode using the PSIM software.



Source: Author

Table 5 – Experiment Parameters - Buck.

Parameter	Value
Input Voltage	V_p = 311 Vpk
Output Voltage	V_o = 250 V
Inductance L	L = 300 μH
Auto Transformer	L_m = 110 μH
Output Capacitor	C_o = 1.34 mF
Filter Inductance	L = 100 μH
Filter Capacitance	C = 1 μF
Switches	SiC CREE C2M0025120
Switching Diodes	SiC
Rectifying Diodes	Ultra Fast
Drivers	FOD 3180
DSP	F28379D Texas Instruments

7 CONCLUSION

This thesis presented a topological variation of a AC-CC Buck-Boost converter applied as a PFC, where a prototype was made in order of ascertain the results. This variation is mainly focused on the implementation of a switching cell and the Pulse-Frequency Modulation (PFM). Those bring several benefits to the usual Buck-Boost, among those are: the ZCZVT which makes the converter more efficient and lighter, due to less losses on switching; the voltage follower characteristic which makes a current loop unnecessary, being so its main benefit. This characteristics make this converter have a simpler and cheaper control loop, due to not needing much computational power.

The objectives that were presented on the introduction were concluded, those objectives were:

• More than 95% efficiency;

This objective was achieved, with the converter demonstrating efficiency up to 96,27%.

• The harmonic values all below the standard EC 61000-3-2;

This objective was achieved, with the harmonic analysis presenting values all below the standard references.

• Power Factor above 0.99.

This objective was achieved, with power factor up to 0.994 on the nominal power output.

• Study the the characteristics of the chosen topology;

This objective was achieved, with a complete analysis of the converter and some of its competitors

• Simulate the converter in order of analysing its behaviour;

This objective was achieved, with a simulation made on PSIM software that represents the behaviour predicted on its study.

• Make a mathematics model of the defined topology;

This objective was achieved, all the equations are presented throughout the thesis.

• Elaborate the control strategy of the closed loop converter;

This objective was achieved, the closed loop was tested in simulation and prototype and is functional.

• Create a prototype and analyse its behaviour;

This objective was achieved, the prototype was built and studied. The tests presented data of the ZCZVT when the switches turn on and the ZVT when the diodes conduct. This switching characteristics bring efficiency gains to the converter, make so that the switches do not need a snubber circuit and that the heat sinkers can be smaller due to lesser losses.

Another characteristic that was analysed is that the frequency on the input inductor is two times the switching frequency, which makes the size of the magnetic core smaller.

Both Buck and Boost operation modes were analysed and the changes that were made on the control system in order to achieve each operation mode are minimal, opening up more possibilities in applications and bringing versatility with simplicity to the converter.

Overall the presented converter bring several advantages to the standard buck-boost topology, presenting gains in size, weight and control complexity, while also presenting the standard characteristics of a PFC. On the other side, this variation brings the need for an extra transformer, which adds to its building complexity and costs, making so that its use is better applied in applications above 1 kW.

7.1 Future Works

Throughout the analysis of the converter studied in this thesis it is possible to see a great potential for developing other studies utilizing the presented information, between several possibilities the ones realized by the author are:

• Parallelism of converters, being so of great use in applications that need redundancies, those could work really well with the control system applied in this converter, which is simple and do not need much processing power to be applied.

• Integration with a second converter in cascade, for utilizing its main application, that is being a PFC.

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APENDIX A – Utilized Code

```c
#include"setup_perifericos.h"
#define BUFFER_SIZE 8
#define DEBUG_OUT1 5

// ADC variables
double adc0 = 0; //ADCINA0 - PV current
double adc1 = 0; //ADCINA1 - BAT current
double adc2 = 0; //ADCINA2 - PV voltage
double adc3 = 0; //ADCINA3 - PV current
double adc4 = 0; //ADCINA4 - BAT voltage

uint16_t adc0_1 = 0;
uint16_t adc0_2 = 0;
uint16_t adc0_3 = 0;
uint16_t adc0_4 = 0;
uint16_t adc0_5 = 0;
uint16_t adc0_6 = 0;
uint16_t adc0_7 = 0;
uint16_t adc0_8 = 0;
double adc0sum = 0;

uint16_t adc1_1 = 0;
uint16_t adc1_2 = 0;
uint16_t adc1_3 = 0;
uint16_t adc1_4 = 0;
uint16_t adc1_5 = 0;
uint16_t adc1_6 = 0;
uint16_t adc1_7 = 0;
uint16_t adc1_8 = 0;
double adc1sum = 0;

uint16_t adc2_1 = 0;
uint16_t adc2_2 = 0;
uint16_t adc2_3 = 0;
uint16_t adc2_4 = 0;
double adc2sum = 0;

uint16_t adc3_1 = 0;
uint16_t adc3_2 = 0;
uint16_t adc3_3 = 0;
uint16_t adc3_4 = 0;
uint16_t adc3_5 = 0;
uint16_t adc3_6 = 0;
uint16_t adc3_7 = 0;
uint16_t adc3_8 = 0;
double adc3sum = 0;

uint16_t adc4_1 = 0;
uint16_t adc4_2 = 0;
uint16_t adc4_3 = 0;
uint16_t adc4_4 = 0;
uint16_t adc4_5 = 0;
uint16_t adc4_6 = 0;
uint16_t adc4_7 = 0;
uint16_t adc4_8 = 0;
double adc4sum = 0;

// Initialize interrupts
__interrupt void isr_cpu_timer0(void);
__interrupt void epwm1_isr(void);
__interrupt void epwm3_isr(void);
__interrupt void epwm4_isr(void);
```

```
 63 __interrupt void isr_adc(void);
 64
 65 // PWM variables
 66 double frequencyKHz;
 67 double epwmfrequency = 410;
 68 double EPWM_MAX_COUNT = 251;
 69 double freq;
 70 double razaoCiclica=0;
 71 double razaoCiclicaB=1;
 72
 73 // control variables
 74 double error0 = 1;
 75 double epwmfrequency1=1050;
 76 double count =0;
 77 int Control_Loop = 0;
 78 //double vref = 1.87337;//1=170,8151
 79 int soft = 0;
 80 int softrep = 0;
 81
 82 double error1=0;
 83 double outputPI;
 84 // Initialize functions
 85 long int i =0;
 86 long int j =0;
 87
 88 void updateSwitching(void);
 89 void ClosedLoopControl(void);
 90
 91
 92 __interrupt void isr_cpu_timer0(void);
 93 __interrupt void isr_adc(void);
 94
 95
 96 void softstarter(void){
 97     while(count <= (800)){
 98         EPwm1Regs.TBPRD = 1600;
 99         EPwm2Regs.TBPRD = 1600;
100         EPwm1Regs.CMPA.bit.CMPA = count;
101         EPwm2Regs.CMPA.bit.CMPA = (1600-count);
102         DELAY_US(5000);
103         count++;
104     }
105 }
106 /**********************************************************************************************
    ************
107  * main.c
108
    **********************************************************************************************
    **********/
109 int main(void){
110     InitSysCtrl();                          // Initialize System Control:
111     InitGpio();
112
113
114
115     DINT;                                   // Disable CPU interrupts
116     InitPieCtrl();                          // Initialize the PIE control registers to
    their default state
117
118
119
120     IER = 0x0000;                           // Disable CPU interrupts
```

```
121     IFR = 0x0000;                           // Clear all CPU interrupt flags:
122     InitPieVectTable();                     // Initialize the PIE vector table
123
124     EALLOW;
125     CpuSysRegs.PCLKCR0.bit.CPUTIMER0 = 1;
126
127
128     PieVectTable.TIMER0_INT = &isr_cpu_timer0;
129     PieVectTable.EPWM3_INT = &epwm3_isr;
130     PieVectTable.EPWM4_INT = &epwm4_isr;
131     PieVectTable.ADCA1_INT = &isr_adc;
132     EDIS;
133
134
135      */
136     // pg. 102 PIE Channel Mapping spruhm8i.pdf - Technical reference
137     PieCtrlRegs.PIEIER1.bit.INTx7 = 1;      // Timer 0
138     PieCtrlRegs.PIEIER3.bit.INTx1 = 1;      // PWM 1
139     PieCtrlRegs.PIEIER3.bit.INTx3 = 1;      // PWM 3
140     PieCtrlRegs.PIEIER3.bit.INTx4 = 1;      // PWM 4
141     PieCtrlRegs.PIEIER1.bit.INTx1 = 1;      //ADC
142     IER |= (M_INT1|M_INT9|M_INT3);
143
144
145     InitCpuTimers();
146     ConfigCpuTimer(&CpuTimer0, 200, 1000000);
147     CpuTimer0Regs.TCR.all = 0x4001;
148
149     Setup_GPIO();
150     Setup_ePWM();
151     Setup_ADC();
152     Setup_DAC();
153
154     if (soft == 1){
155           softstarter();
156        }
157
158     EINT;                                   // Enable Global interrupt INTM
159     ERTM;                                   // Enable Global realtime interrupt DBGM
160
161     while(1){
162
163
164     }
165
166
167
168 }
169
170
171 /*************************************************************************************************
    ***********
172  * Interrupts functions
173
    *************************************************************************************************
    **********/
174
175 __interrupt void isr_cpu_timer0(void){
176     //interrupt timer 0
177     //GpioDataRegs.GPATOGGLE.bit.GPIO31 = 1;
178     PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
179 }
```

```
180
181
182
183 __interrupt void epwm3_isr(void)
184 {
185
186     EPwm3Regs.ETCLR.bit.INT = 1;
187     PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
188     AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1;      //Clear ADC Interrupt flag
189
190 }
191
192 __interrupt void epwm4_isr(void){
193
194     if(Control_Loop == 1){
195           ClosedLoopControl();
196        }
197
198     GpioDataRegs.GPADAT.bit.GPIO14 = 1;
199     updateSwitching();
200     GpioDataRegs.GPADAT.bit.GPIO14 = 0;
201     EPwm4Regs.ETCLR.bit.INT = 1;
202     PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
203
204 }
205
206 __interrupt void isr_adc(void){
207
208
209     //ADCINA0 - Battery current
210     adc0_8 = adc0_7;
211     adc0_7 = adc0_6;
212     adc0_6 = adc0_5;
213     adc0_5 = adc0_4;
214     adc0_4 = adc0_3;
215     adc0_3 = adc0_2;
216     adc0_2 = adc0_1;
217     adc0_1 = 0;//AdcaResultRegs.ADCRESULT0;
218     adc0sum = (adc0_1+adc0_2+adc0_3+adc0_4+adc0_5+adc0_6+adc0_7+adc0_8)*0.125;
219     adc0 = adc0sum/1240.909091;
220
221     //ADCINA1 - Battery current
222     adc1_8 = adc1_7;
223     adc1_7 = adc1_6;
224     adc1_6 = adc1_5;
225     adc1_5 = adc1_4;
226     adc1_4 = adc1_3;
227     adc1_3 = adc1_2;
228     adc1_2 = adc1_1;
229     adc1_1 = AdcaResultRegs.ADCRESULT1;
230     adc1sum = (adc1_1+adc1_2+adc1_3+adc1_4+adc1_5+adc1_6+adc1_7+adc1_8)*0.125;
231     adc1 = (adc1sum/1240.909091)*167.973;//202.573;
232
233
234     AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1;      //clear INT1 flag
235     PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
236     //GpioDataRegs.GPADAT.bit.GPIO14 = 0;
237 }
238
239 /*************************************************************************************
    ************
240  * User Programmed Functions
```

```
241 ***********************************************************************************************
    **********/
242
243
244
245 void updateSwitching(){
246
247
248     EPwm1Regs.TBPRD = epwmfrequency;               // Set timer period
249     EPwm1Regs.CMPA.bit.CMPA = epwmfrequency/3;     // Duty Cycle
250
251     freq = (50000.0/epwmfrequency);
252
253     EPwm2Regs.TBPRD = epwmfrequency;               // Set timer period
254     EPwm2Regs.CMPA.bit.CMPA = epwmfrequency/2;     // Duty Cycle
255
256     freq = (50000.0/epwmfrequency);
257     AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1;
258
259
260
261
262 }
263
264
265 double ta=1/20000;
266 double result;
267 double kp = 9.52e-6; //kp = 3.29999909e-5
268 double ki = 5.5e-13; //ki = 0.50000009e-12
269
270
271 double mi0 = 0;
272 double mi1 = 0;
273 double ts = (1/20000);
274 double pi = (1/50000);
275 double pi1 = (1/50000);
276 double proportional;
277 double integrator;
278 double integrator1=0;
279 double frequency = 50000;
280 double frequency1 =50000;
281 double outputDAC=0;
282 double vref = 200;//320
283 double result1 =0;
284 double integral=0;
285 double integral1=0;
286
287 void ClosedLoopControl(){
288
289     error1= error0;
290     error0 = ((vref-adc1));
291
292    integral1 = integral;
293    integral = error0*ki+integral1;
294    integrator = integral;
295    proportional = (kp*error0);
296
297    pi= integrator + proportional;
298
299
300  if (integral>0.0000310)integral = 0.0000310;
```

```
301 if (integral<(-0.00000405))integral = -0.00000405;
302 result = 1/pi;
303
304    frequency1 = 1/pi;
305    frequency = frequency1;
306    epwmfrequency1 = (50000/frequency)*1000;
307
308           if (frequency < 32000) epwmfrequency1 = 1540;
309           if (frequency > 250000) epwmfrequency1 = 201;
310           if(frequency1<32000) frequency1 = 32000;
311
312            epwmfrequency = epwmfrequency1;
313
314            outputDAC=adc1sum;
315            EALLOW;
316            DacaRegs.DACVALS.bit.DACVALS = outputDAC; //12 bits
317            EDIS;
318 }
319
320
321
322
323
324
325
326
327
328
329
330
331
```

Figure 40 – Code for the control loop.

```
286
287 void ClosedLoopControl(){
288
289     error1= error0;
290     error0 = ((vref-adc1));
291
292    integral1 = integral;
293    integral = error0*ki+integral1;
294    integrator = integral;
295    proportional = (kp*error0);
296
297    pi= integrator + proportional;
298
299
300  if (integral>0.0000310)integral = 0.0000310;
301  if (integral<(-0.00000405))integral = -0.00000405;
302  result = 1/pi;
303
304     frequency1 = 1/pi;
305     frequency = frequency1;
306     epwmfrequency1 = (50000/frequency)*1000;
307
308           if (frequency < 32000) epwmfrequency1 = 1540;
309           if (frequency > 250000) epwmfrequency1 = 201;
310           if(frequency1<32000) frequency1 = 32000;
311
312            epwmfrequency = epwmfrequency1;
313
314            outputDAC=adc1sum;
315            EALLOW;
316            DacaRegs.DACVALS.bit.DACVALS = outputDAC; //12 bits
317            EDIS;
318 }
```

Source: Author